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MICROELECTRONICS RESEARCH FOR SHUTTLE AND SPACE STATION

RESEARCH ACHIEVEMENTS REVIEW

VOLUME III REPORT NO. 11

SCIENCE AND ENGINEERING DIRECTORATE
GEORGE C. MARSHALL SPACE FLIGHT CENTER
MARSHALL SPACE FLIGHT CENTER, ALABAMA

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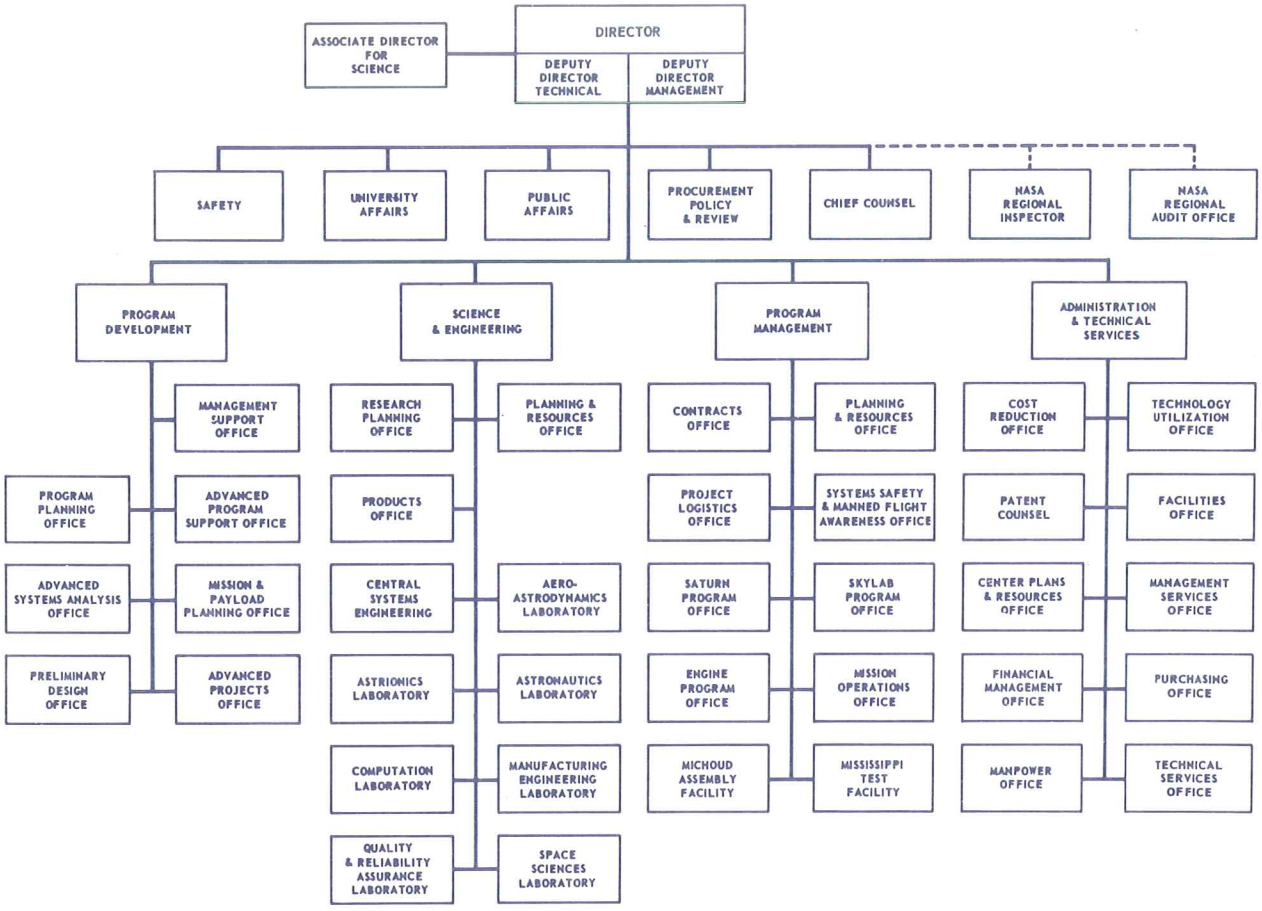

RESEARCH ACHIEVEMENTS REVIEWS COVER THE FOLLOWING FIELDS OF RESEARCH

- Radiation Physics
- Thermophysics
- Chemical Propulsion
- Cryogenic Technology
- Electronics
- Control Systems
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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

WASHINGTON, D. C.

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PREFACE

In February, 1965, Dr. Ernst Stuhlinger, now Marshall Space Flight Center's Associate Director for Science, initiated a series of Research Achievements Reviews which set forth those achievements accomplished by the laboratories of the Marshall Space Flight Center. Each review covered one or two fields of research in a form readily usable by specialists, systems engineers and program managers. The review of February 24, 1966, completed this series. Each review was documented in the "Research Achievements Review Series."

In March, 1966, a second series of Research Achievements Reviews was initiated. This second series emphasized research areas of greatest concentration of effort, of most rapid progress, or of most pertinent interest and was published as "Research Achievements Review Reports, Volume II." Volume II covered the reviews from March, 1966, through February, 1968.

This third series of Research Achievements Reviews was begun in March, 1968, and continues the concept introduced in the second series. Reviews of the third series are designated Volume III and will span the period from March, 1968, through March, 1970.

The papers in this report were presented January 29, 1970

William G. Johnson
Director
Research Planning Office

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MICROELECTRONICS RESEARCH AND TECHNOLOGY FOR SHUTTLE AND SPACE STATION

By

D. L. Anderson

INTRODUCTION

Electronics is in the midst of a revolution. The pace at which electronics changes and its impact on related fields such as military and space systems, medicine, and computer technology make it one of the most exciting of the technical fields. Progress is so rapid that it is impossible for even a dedicated electronics engineer to stay abreast of its many facets.

By observing advances occurring during the last three decades, some of the happenings to occur in the fourth decade of the revolution and how they will influence Shuttle and Space Station electronic systems can be projected. Table 1 shows the dominant amplifying or functional component used in each decade. Table 2 provides more detail on the developments, fallout, and breakthroughs of each. A similarity exists in occurrences of the first three decades; i.e., a technology develops, there are important commercial and industrial fallouts, and a breakthrough occurs toward the end of each decade that spurs action in the next. As for the 1970 to 1980 decade, it can be predicted that large scale integrated circuits (LSI) will play the dominant role in new systems. It is almost certain that LSI will spawn great computers that will be influencing our lives before the end of the decade. There are some very sophisticated and demanding electronics systems to be developed, and LSI is the tool to be used in meeting these goals. It would be foolish at this time to try to predict a breakthrough in the late 1970's; but with research underway throughout the industry, it probably will occur.

TABLE 1. PRINCIPAL AMPLIFYING OR FUNCTIONAL COMPONENT BY DECADE

1940 to 1950	Vacuum Tube
1950 to 1960	Transistor
1960 to 1970	Integrated Circuit
1970 to 1980	Large Scale Integrated Circuit

APPLYING MICROELECTRONIC TECHNOLOGY TO THE SHUTTLE AND SPACE STATION

Large scale integration does not exist in all the needed forms, and its applications to systems pose many new problems for engineers. The following areas are those in which effort is being applied to make the latest in microelectronic development available for use in the Shuttle and Space Station.

Engineering Evaluation and Testing of LSI Chips

There are many technologies by which LSI chips may be manufactured. Bipolar, p-channel metal oxide semiconductor (MOS) (P-MOS), n-channel MOS (N-MOS), and complementary MOS (C-MOS) are a few, and there are variations of each of these. These technologies differ in speed, power consumption, cost, packing density, and inherent reliability. It is therefore imperative that an evaluation of the various types be performed for Shuttle and Space Station applications. In addition, the functional testing of large logic arrays becomes a formidable task and can only be accomplished by complex test equipment using computers. The areas of evaluation and testing are extremely important ones and are receiving attention.

Design and Development of Custom Chips

The fact that LSI makes it possible to put much larger circuits on one chip results in more of the chips being custom. This slows procurement of the needed circuits since they must first be developed. An in-house capability for computer-aided design and mask making is being developed at MSFC to speed up the process. Interface with industry can be accomplished at any point from logic design to supplying finished masks for circuit fabrication.

TABLE 2. THE FOUR DECADES OF ELECTRONICS

1940 to 1950
- a. Development: Sophisticated electronic circuits for radar and other military electronic systems using vacuum tubes.
- b. Fallout: Home television and early vacuum tube computers.
- c. Breakthrough: The transistor made its debut in 1948.

1950 to 1960
- a. Development: Advanced solid-state circuits for space and military applications.
- b. Fallout: Reliable, high speed commercial computers. Japanese transistor radios.
- c. Breakthrough: The monolithic integrated circuit was invented late in the 1950's.

1960 to 1970
- a. Development: Application of integrated circuits making more complex electronic systems possible.
- b. Fallout: Larger, higher speed computers became available.
- c. Breakthrough: Large scale integrated circuits became a reality late in the 1960's.

1970 to 1980
- a. Development: Application of LSI to very complex military and space systems.
- b. Fallout: Giant commercial computers and data handling systems. Near maintenance-free home electronics.
- c. Breakthrough: ?

Application of LSI to Electronic Systems

LSI spans several technologies such as P-MOS, C-MOS, and bipolar technologies. Each has its advantages and disadvantages. This gives the design engineer a wide choice of approaches for solving his problems but also complicates matters. However, by proper selections, interfacing, and partitioning, far more complex systems can be designed and fabricated than were possible a few years ago.

Advanced Packaging Technology

Small size, light weight, low power, and long trouble free life are inherent characteristics of large scale integrated electronics. LSI, however, applies only to the semiconductor chip. The assembly of complete electronic systems requires a technology for interconnecting chips and other electronic parts on common substrates. It is here that hybrid microelectronic technology admirably fills the need. Thick and/or thin films are deposited on ceramic substrates to form electronic parts and interconnection systems. The combination of LSI and hybrid microcircuit techniques provides the means for meeting the demanding requirements of Shuttle and Space Station electronic systems. MSFC's capability in this area is extensive, and new methods are presently being developed.

Long Life and Reliability

Just as integrated circuits increased the reliability of electronic systems by incorporating more circuitry in a chip and decreasing the numbers of bonds, LSI will increase reliability even further. The proof of reliability by the numbers was complicated by the integrated circuit, because it was no longer possible to conduct the exhaustive tests needed to obtain realistic mean-times-to-failure. LSI makes the number game even more difficult. New accelerated test methods are needed to get the best information possible for reliability purposes.

Another approach to more reliable parts is line certification. By carefully inspecting and approving the lines on which parts are made and performing 100-percent screening, it is possible to achieve a greater degree of reliability than has been enjoyed in the past.

Application of Computers to Design, Layout, and Testing of LSI Arrays

Three to four man-months are required to design and thoroughly check the artwork for a complex MOS/LSI array of several thousand transistors. This is not an unreasonable requirement for a chip going into heavy production of hundreds of thousands of units. For custom circuits, however, more efficient design procedures are required. The use of computers in design and testing is being used throughout industry and a program is underway in the Astrionics Laboratory of MSFC to improve computer-aided design capability to meet the demanding requirements.

REVIEW PAPERS

The papers chosen for this review represent a broad spectrum of activities. There are two papers in each of four basic areas: the first two discuss aspects of hybrid microelectronic technology; the third and fourth are related to LSI arrays; the fifth and sixth represent efforts in applying microelectronics to systems; and the seventh and eighth are concerned with the quality and reliability aspects of microelectronics. These areas have been touched on above in a broad sense; but the following papers will go into greater detail on the selected subjects.

DEVELOPMENT OF TRIMMING TECHNIQUES FOR MICROCIRCUIT THICK-FILM AND THIN-FILM RESISTORS

By

S. V. Caruso and R. V. Allen*

SUMMARY

Thick-film and thin-film resistors contained in hybrid microcircuits normally require adjustment for precision tolerances of ±1 percent or better. Current trimming techniques were evaluated and are discussed. The air-abrasive method was determined to be best for thick films. Laser trimming and ultrasonic trimming were found to be most successful with thin films. A hybrid microelectronic development program and resistor trimming results are presented.

INTRODUCTION

Hybrid Microelectronics

Hybrid microcircuit technology is rapidly becoming a standard technique in electronic hardware development and fabrication. It is predicted that this technology should become the prime assembly method of most high volume electronic circuit production lines. Already, major device manufacturers, systems houses, and many new companies are converting to or specializing in microelectronics. The most obvious reasons are products of small size and high reliability. Great advances are currently being made in the development of simple (transistors, diodes) and complex (MSI, LSI, IC's) monolithic devices. The hybrid technology is simply a method of putting together (or packaging) total circuits and systems. As defined, a hybrid is a microcircuit fabricated on an insulating substrate using some combination of film elements, monolithic chips, and discrete components. Figure 1 is an example of a typical hybrid microcircuit. This particular circuit functions as a power supply and is a modular part of a microelectronic accelerometer sensing system.

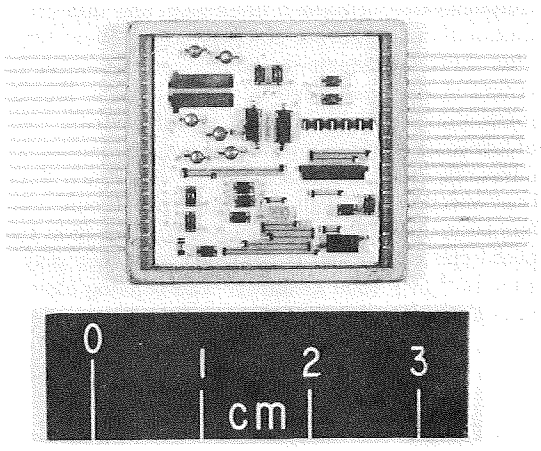

Figure 1. Hybrid microelectronic circuit.

Marshall Space Flight Center Application

Marshall Space Flight Center (MSFC) conducts in-house research on the development and fabrication of hybrid microcircuits and builds prototypes for feasibility study. A typical applications program conducted at MSFC was the design and fabrication of the hybrid accelerometer system.

The Saturn IB booster vehicles, developed at MSFC, contain an accelerometer system in the instrumentation unit structure. This system has two functions during flight of the vehicle: (1) sense lateral acceleration of the vehicle caused by high aerodynamic loading pressures and jetstream winds encountered during first-stage burn and (2) condition the lateral acceleration information and make it available to the vehicle control system to control

*The authors wish to acknowledge the assistance of Mr. M. L. Yongue, Mr. J. B. Farner, and Mr. J. B. Besherse in actually fabricating and trimming the microcircuits tested.

angle-of-attack. Electrically, the system senses acceleration as an input, operates with dc voltage, and provides a dc output proportional to the acceleration sensed. The applications for a microelectronic version of the accelerometer are on vehicles that are weight- and size-limited and for the increased reliability inherent with microelectronic hardware.

The electronic circuitry used in the conventional hardware was redesigned and then fabricated as a hybrid microcircuit assembly. The subsystems were packaged in 2.54 by 2.54 cm (1.0 by 1.0 inch) flatpacks that contained thick-film and thin-film elements and discrete components. Seven flatpacks plus three transformers comprised the entire electronic system and were interconnected in modular form using weldable printed circuit boards. The electronics of the conventional accelerometer are currently packaged in a 1.0 ℓ (1×10^{-3} m^3) "black box" weighing 1.8 kg. The microelectronic assembly has been completed and electrically tested in the prototype stages and is designed to occupy only 0.3 ℓ (3×10^{-4} m^3) (500 grams). The sensing element is common to both designs.

MICROCIRCUIT FABRICATION

A typical hybrid microcircuit fabrication process uses a thick-film conductive paste, silk-screened onto a glazed alumina substrate, dried at 373.15°K (100°C), and fired at approximately 923.15°K (650°C). The thick film serves as a conductive network and as weld pads for discrete components and wire leads. After firing, the substrate is placed in a vacuum system and thin-film resistors, capacitors, and conductors are vapor-deposited onto the substrate. The configuration of the thin-film elements is defined by metal masks placed in near contact with the substrate. The substrate size is a standard 5.08 by 5.08 by 0.635 cm (2.0 by 2.0 by 0.025 inch) during processing and is scribed and broken to final size for placement into the package. Discrete components are bonded to the substrate, and leads are then joined to the proper terminals. The complete circuit is mounted in a package, such as a 2.54 by 2.54 cm (1.0 by 1.0 inch) metal flatpack, and then hermetically sealed with a metal cover.

Film Resistors

The complexity of developing and producing microcircuits is seen from viewing the simple circuit as shown in Figure 1. Therefore, this presentation will be limited to one of the many components used in hybrid integrated circuits; that is, the film resistor.

The advantages gained by using integrated circuits (IC) are numerous and have been expounded over the past several years. Without enumerating all the merits of IC's, the most obvious advantage is increased reliability through the use of solid-state components (transistors, diodes, monolithic integrated circuits, resistors, and capacitors).

Two factors must be considered when contemplating the design and use of hybrid microcircuits; first, the resistance tolerances that can be achieved in fabrication; and, second, the possibility of changing the resistance values of the circuit after production.

Discrete resistors in conventional electronics such as printed circuit boards can be selected and connected into a circuit without affecting the value of other components; however, thick-film and thin-film resistors are intimately interconnected to other components on a common substrate. This makes it necessary to hold resistance tolerances as close as possible during the fabrication process. However, to obtain a higher degree of precision than is possible by the fabrication process, resistors must be adjusted by trimming after they are formed. It would appear at first glance that undue importance is being attached to a single type of component; that is, a resistor. However, in the design of microcircuits, resistor layout normally dictates the assembly criteria for the total electronic package. The two types of resistors of interest to this discussion are thin-film vacuum deposited resistors and thick-film screened resistors.

RESISTOR TRIMMING METHODS

As mentioned previously, film resistors are formed on a substrate by both thin-film vacuum deposition and thick-film paste screening. The tolerance to which a resistor is manufactured depends

on such factors as fabrication method, material, and operator skill. A typical film resistor is shown in Figure 2.

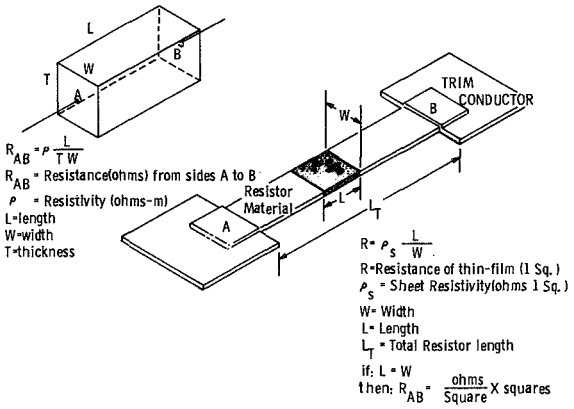

Figure 2. View of a typical film resistor.

As a general rule, thin-film resistors can be deposited through precision masks to a tolerance of ±3 to ±5 percent and photoetched to a tolerance of ±10 percent. Thick-film resistors can be screened to an as-fired tolerance of ±20 percent. In any event, when better than ±3 percent precision is required, it must be obtained through the proper trimming technique.

Table 1 provides a summary of information that is pertinent to resistor materials that are most often used in hybrid circuits.

A number of trimming techniques have been developed for adjusting the value of resistors after they are formed on the substrate. The most commonly used techniques are shown in Table 2.

The physical layout of resistors in a circuit takes into consideration the requirement for postdeposition adjustment. For example, Figure 3 indicates methods of design that facilitate resistor trimming.

Figure 4 illustrates one technique by which resistors are trimmed and will be discussed in this report. The darkened square on the left represents an area of the original resistor width. By reducing the width along a given length of the film resistor, the number of squares is increased, thus increasing the total resistance. This follows, since the resistivity or ohms-per-square value remains unchanged.

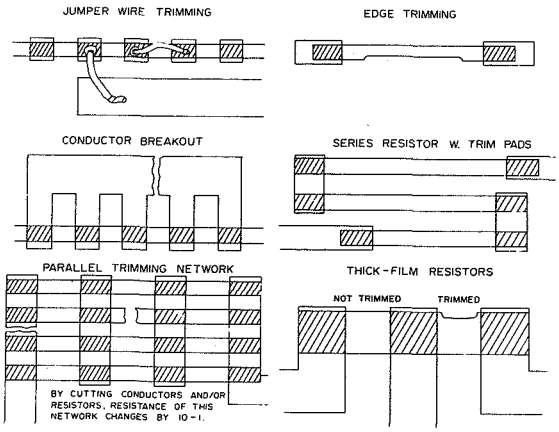

Figure 3. Resistor layout methods.

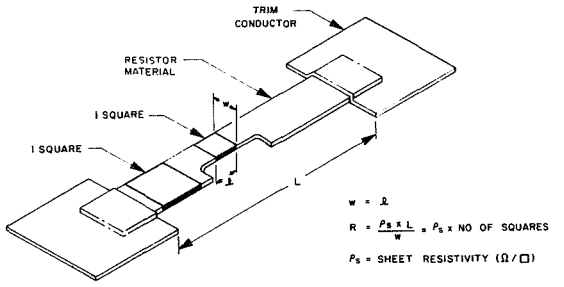

Figure 4. Thin-film resistor trimming.

Equipment and Techniques

Two resistor trimming methods were selected for use on thin-film circuits produced in the Astrionics Laboratory of MSFC; laser trimming and ultrasonic trimming.

LASER TRIMMING

The laser, in some respects, is an ideal tool for this application. Material can be removed from a resistor without causing damage to the substrate and contaminating other parts of the circuit.

The laser shown in Figure 5, used for circuit trimming, consists of a laser head, a power supply and a microscope. The laser head contains a ruby rod that emits light at a wavelength of 6943×10^{-10} m (6943 Å) and a pulse length of 150 μsec with maximum power output of 300 mJ. The repetition rate

TABLE 1. RESISTOR MATERIAL INFORMATION

Resistors	Composition	Resistivity Range (ohms per square)	Temp. Coefficient of Resistance (ppm/°C)	Deposition Technique	As Deposited Tolerances
Thin Film:				(Notes)	
Nichrome V	80% Ni-20% Cr.	50 to 500	0 to ±30	1, 2, 3	±3 to ±10%
Chromel C	74% Ni-20% Cr. -6% Fe	50 to 500	50 to 100	1, 2, 3	±3 to ±10%
Dielectric-Metal (Cermets)	SiO-Cr, SiO-Ni TiN-Cr	0.050k to 10k	>200	1, 2, 3	±20%
Tantalum Oxide	TaO	0.050k to 10k	>200	3 (Reactive) (RF)	±20%
Tantalum Nitride	TaN	0.050k to 1M	>200	3 (Reactive) (RF)	±20%
Thick Films	PdO, AgO-Glass Frit-Cermets	0.10k to 1M	100 to 500	Silk Screen	±10 to ±20%

Notes:
1. Resistance Heating
2. Electron Beam
3. Sputtering

TABLE 2. RESISTOR TRIMMING TECHNIQUES

Trimming Method	Applicable Resistor Type		Tolerance Attainable	Advantages	Disadvantages
	Thin-Film	Thick-Film			
1. Electrical Pulse	X		0.01%	a. Precision Resistors b. Automatic c. Clean	a. Extremely Thin $<10^{-8}$ m (100 Å) b. Individual Trim c. Oxidized Film
2. Thermal	X		0.01%	(Same as 1)	(Same as 1)
3. Mechanical Scribe	X		1.0%	a. Inexpensive Equipment	a. Manual (Slow)
		X	3.0%		b. Non-Reproducible c. Substrate Damage d. Particulate Contamination
4. Ultrasonic	X		0.1%	a. Precise Resistors	a. Substrate Damage
		X	1.0%	b. Automatic c. Fast	b. Particulate Contamination
5. Laser	X		0.01%	(Same as 4)	a. Laser Safety Hazard
		X	0.1%	d. Clean ?	b. Slow c. Expensive
6. Abrasive		X	0.1%	a. Precision Resistors b. Automatic c. High Volume d. Inexpensive	a. Particulate Contamination b. Substrate Recleaning
7. Chemical Etch	X		2%		a. Chemical Exposure b. Slow (Several Steps) c. Cleaning Required d. Residue Possible

Figure 5. Laser trimming equipment.

is 1 pulse per 15 sec with nitrogen cooling. The spot size is adjustable from 10^{-6} to 12.7×10^{-5} m (1μ to 5 mils). A functional diagram is shown in Figure 6.

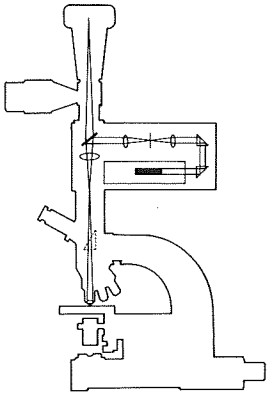

Figure 6. Laser trimmer diagram.

Figure 7 shows some actual thin-film circuits trimmed with the laser. Although not a subject in this report, thin-film capacitors have been successfully trimmed using this laser technique. The three resistors shown have been trimmed by varying the trimming width. In actual application, the maximum reduction of width allowed is 30 percent. For circuits that were laser-trimmed, a passivation protective film of silicon monoxide is deposited over the resistors during the initial deposition. This technique assures that the thin-film metal resistors are never exposed to the atmosphere. The laser trims the resistors through the silicon-monoxide coating.

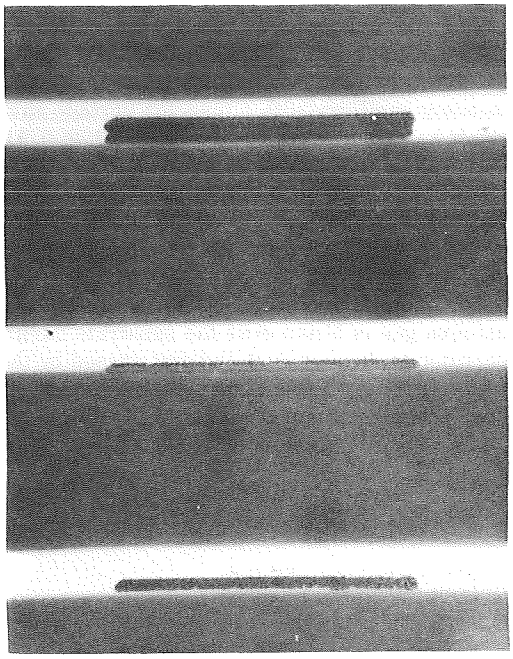

Figure 7. Laser trimmed thin films.

ULTRASONIC TRIMMING

Ultrasonic trimming is the second technique used in our laboratory to adjust the values of deposited resistors. The ultrasonic trimming technique is a process by which material is removed from a thin-film resistor line by friction contact of a hard metal probe (Fig. 8). The apparatus is a standard conventional ultrasonic bonder capable of bonding small

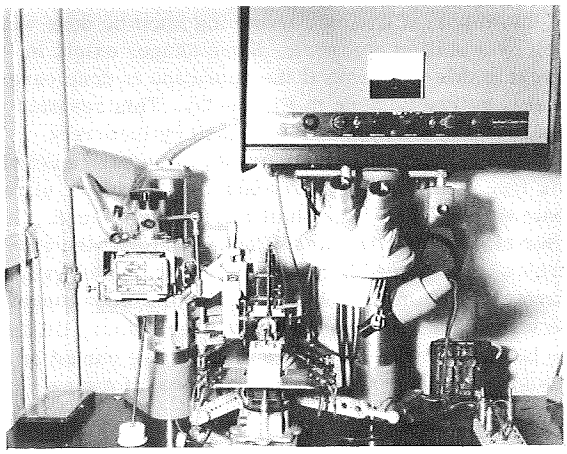

Figure 8. Ultrasonic trimming equipment.

diameter gold and aluminum wire for interconnections on monolithic and hybrid circuits. The conversion to a trimming tool consists of replacing the wire bonding capillary with a tungsten carbide shaft. This shaft has a machined flat tip of 0.005 by 0.013 cm (0.002 by 0.005 inch). The flat surface of this shaft is placed on the edge of the resistor and, when vibrated ultrasonically, removes the film beneath the tip. By moving the tip along the edge of the resistor, material is thus removed until a pre-set resistance value is achieved. A steady stream of dry nitrogen gas is blown over the substrate during the operation to remove dust and grit caused by the ultrasonic action. Figure 9 shows some thin-film resistors trimmed and untrimmed.

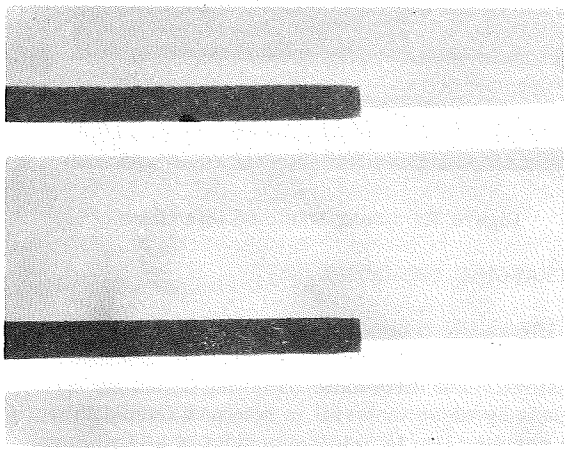

Figure 9. Ultrasonic trimmed thin films.

However, ultrasonic trimming must be done with care by a skilled operator. Some danger exists in cracking this substrate if the operation is done carelessly, as can be seen in Figure 10. This resistor line contains a chipped area caused by incorrect placement of the ultrasonic probe. Another cause of this type catastrophy is premature firing of the ultrasonic energy before the shaft is properly placed. After ultrasonic trimming of the resistors, the substrates were placed back in the vacuum system where a protection film ($\sim 10^{-8}$; ~ 100 Å) of silicon monoxide was deposited over the resistor surfaces. Unlike the laser technique, the silicon monoxide cannot be deposited on the resistors prior to the trimming operation.

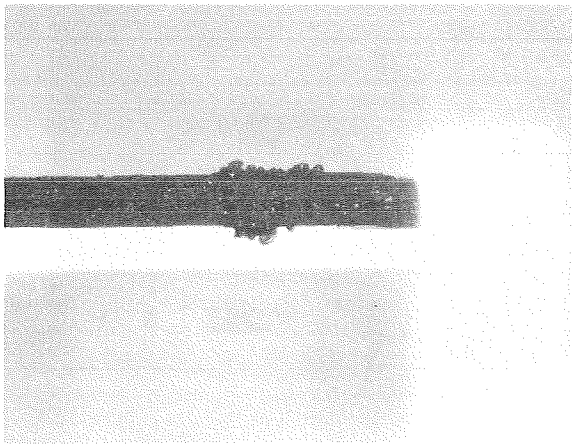

Figure 10. Thin-film resistor damaged by ultrasonic trimming.

QUALITY AND RELIABILITY REQUIREMENTS

One of the prime considerations for electronic hardware is long life reliability (10- to 14-year missions). As pointed out in the variety of trimming methods available, there are advantages and disadvantages for each technique. The selection of trimming procedures for our laboratory, therefore, was based on a number of criteria: (1) the methods must be reasonably economical; (2) a technician should be able to operate the equipment with reproducible results; and, probably most important, (3) the substrate, resistors, and, where applicable, discrete components must show no physical damage or particle contamination as a result of the trimming operation; that is, the circuits must pass visual inspection during normal processing. Of course, there will be a physical change in the resistor since adjustment normally requires removal of material. In essence, the program being described can be classified as a reliability study for the determination of confidence level in the selected techniques.

To determine the confidence level of these methods in terms of long term reliability, an evaluation of the previously described trimming methods was conducted. Thin-film resistors were deposited

on a glazed ceramic substrate to a resistivity of 200 ohms per square. The resistors were vapor deposited at a pressure of 13.33×10^{-5} N/m^2 (10^{-6} torr) and consisted of an alloy material of 20 percent chromium and 80 percent nickel (Nichrome V).

The test samples were divided into three groups (Table 3): (1) control samples, (2) laser trimmed samples, and (3) ultrasonically trimmed samples. Each group contained six substrates with six resistors per substrate ranging in value from 6.2 to 130 kilohms. Each group was subjected to temperature aging, temperature-cycling, and load-life tests.

Test Procedures

TEMPERATURE-AGING TEST

The purpose of the temperature aging test was to determine the effects on the resistance of thin-film resistors resulting from an elevated ambient temperature for a prolonged period of time. The resistors were tested under a no-load condition. All resistance measurements were made at a temperature of 298.15°K (25°C).

TEMPERATURE-CYCLING TEST

The temperature cycling test was to determine the behavior of thin-film trimmed and untrimmed resistors to short periods of thermal shock. One test cycle consisted of subjection of the trimmed and untrimmed samples to a temperature of 218.15°K (-55°C) for 15 minutes, 298.15°K (25°C) for 10 minutes, 398.15°K (125°C) for 15 minutes, and 298.15°K (25°C) for 10 minutes. This cycle was repeated 100 times.

LOAD-LIFE TEST

The purpose of the load-life test was to determine the effects on the electrical and mechanical durability of trimmed and untrimmed resistors when subjected to elevated temperature and loaded to the maximum rated power dissipation. The resistor samples tested were subjected to a temperature of 398.15°K (125°C) for 2000 hours. Each resistor was loaded to 100 mW.

Test Results

VISUAL INSPECTION

A visual inspection was conducted on the substrate, resistors, etc., and there appeared to be no evidence of damage in the areas that were trimmed. Changes in resistance values during environmental tests were very slight and could be attributed to normal drift of the components under the test conditions (as evidenced by the control samples).

TEST DATA

Results of the temperature aging, temperature cycling, and load life tests are shown in Figures 11, 12, and 13. Each point on the curves represents an average value for a set of resistors of the same resistance range. Obviously, these figures show only a representative sampling of the total resistors tested. However, these curves are typical of the test results. No catastrophic failures or unusual resistance changes were experienced during the entire program.

TABLE 3. RESISTOR TRIMMING PROGRAM OUTLINE

Trimming Method	Load Life (100 mW)	Temperature Age [398.15°K/2000 hrs (125°C/2000 hrs)]	Temperature Cycle (100) [218.15°K to 398.15°K (-55°C to +125°C)]
Control	(2)[a] [12][b]	(2) [12]	(2) [12]
Laser	(2) [12]	(2) [12]	(2) [12]
Ultrasonic	(2) [12]	(2) [12]	(2) [12]

a. ( ) — Indicates Number of Substrates Tested
b. [ ] — Indicates Total Number of Resistors

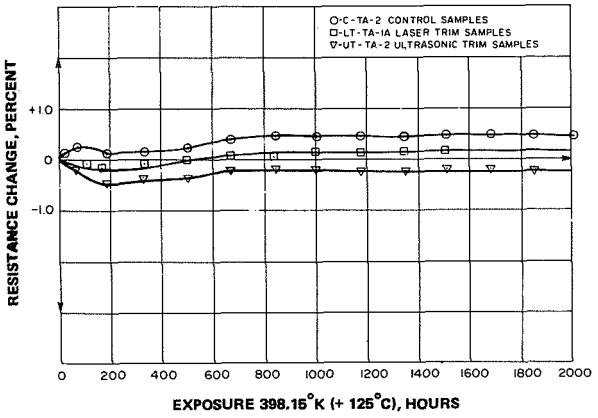

Figure 11. Temperature aging results.

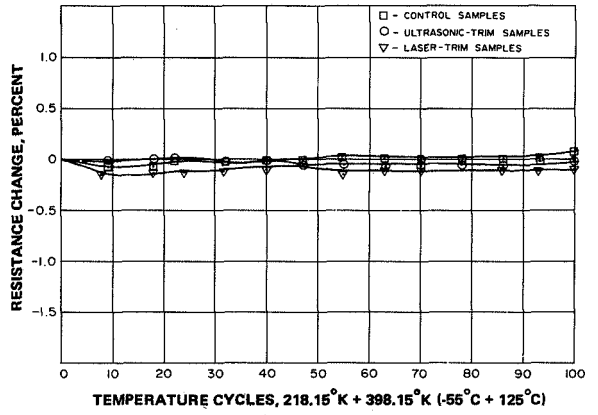

Figure 12. Temperature cycling results.

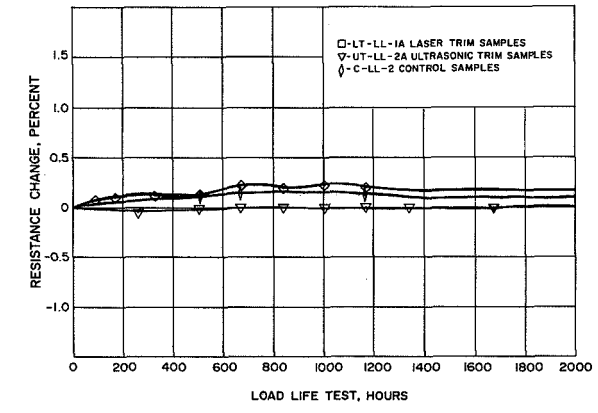

Figure 13. Load life test results.

CONCLUSIONS

To make hybrid circuits attractive for microelectronic applications, film resistor values must be capable of being adjusted after they are formed on the substrate. Tolerances of ±1 percent must be obtainable. The basic mechanism for trimming resistors is relatively simple and, as mentioned earlier, requires physically removing material or oxidizing the resistor by electrical pulse or methods that provide elevated temperature to the film. However, the difficult part of this operation is to accomplish trimming without damaging and/or contaminating the substrate. The data evolved from this test program proved that laser trimming is the highest quality method to use for thin-film resistors. However, laser trimming is slow. Ultrasonic trimming is relatively fast and does scratch the substrate, but is usable without apparent permanent damage to the resistors. As with any technique, final application dictates the requirements and criteria used in a given fabrication process. Lasers are accurate and clean, but slow (fast repetition lasers are available but very expensive). Ultrasonic trimming is fast, with medium accuracy, but does scratch the substrate. Both techniques have been used successfully and, when properly applied, had no detrimental effects on the circuit.

Trimming thick-film resistors (screen process) is routinely accomplished using air-abrasive techniques. Because of the ceramic-like nature of the materials, the substrate can be cleaned after trimming. Although other methods can and do work on thick films, air-abrasion trimming is the most economical and fastest.

DEVELOPMENT AND FABRICATION OF A MICROELECTRONIC CONTROL ACCELEROMETER SYSTEM

By

R. V. Allen, S. V. Caruso, G. L. Filip, and R. F. DeHaye*

SUMMARY

A flight control accelerometer used on the Saturn IB vehicle was redesigned and packaged using hybrid microcircuit technology. Though there is currently no requirement for use of this control accelerometer on the Saturn V vehicles, the design, fabrication, and packaging of this system has proven the feasibility of such applications. Experience gained by the Hybrid Microelectronics Research Section of the Astrionics Laboratory of Marshall Space Flight Center in the course of this project has greatly advanced the capabilities of the Section and contributed to the state-of-the-art.

INTRODUCTION

In the past few years, hybrid microcircuit technology has become a standard technique in the development and fabrication of electronics hardware. This technique is basically a method of packaging circuits and systems to realize the advantages of weight and size reduction, and the associated high reliability factor. Figure 1 illustrates a typical microcircuit.

The Hybrid Microelectronics Research Section serves as a prototype and research facility for Astrionics Laboratory at Marshall Space Flight Center, with basic responsibility for investigating the feasibility of producing circuits and systems using hybrid technology. In addition, this section performs basic research on thin- and thick-film materials and processes, and assists in the monitoring and control of hybrid microcircuit contracts awarded by MSFC.

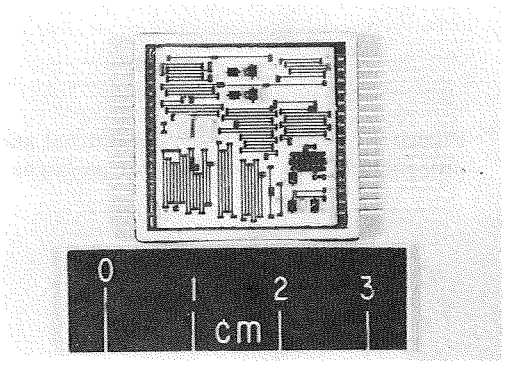

Figure 1. Typical microcircuit.

One project completed by the Section was the design and fabrication of a flight control accelerometer using hybrid microcircuits to reduce the size and weight, update the electronics hardware, and increase the reliability factor.

FLIGHT CONTROL ACCELEROMETER

Function

The flight control accelerometer chosen for redesign had been flown successfully on the Saturn IB vehicles. Figures 2 and 3 provide a comparison of the conventional and microelectronic control accelerometer packages.

The flight control accelerometer is used to sense lateral accelerations of the vehicle caused by high aerodynamic loading pressures and jet stream winds encountered during first stage burn. The accelerometer conditions the lateral

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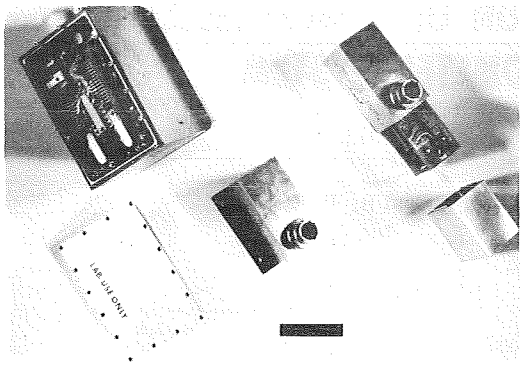


Figure 2. Comparison of conventional and microelectronic accelerometer packages.

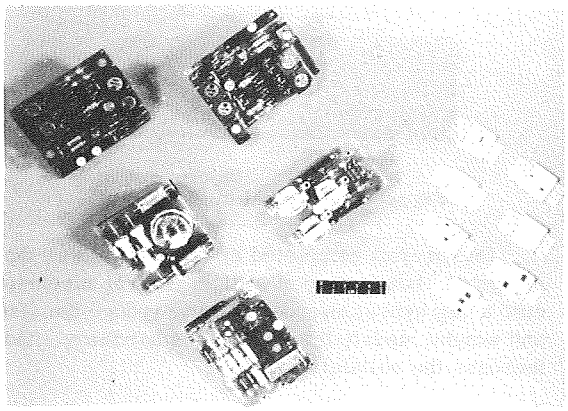


Figure 3. Comparison of conventional and microelectronic accelerometer electronics.

acceleration information and makes this information available to the vehicle control system. Using this information, the vehicle control system controls the vehicle angle-of-attack.

The basic element of the accelerometer is the sensor. The sensor is a transducer that converts the lateral accelerations of the vehicle into electrical signals. The sensor contains a critically suspended weight, or seismic mass, which is affected by movement and produces a corresponding change in the inductive coupling between the primary and secondary windings of a coil, also contained in the sensor assembly. The resulting ac output from the sensor is directly proportional to the magnitude of the lateral acceleration of the vehicle. The ac signals from the sensor are amplified and converted to dc signals which are applied to the flight control computer. The flight control computer uses inputs from the accelerometers, in addition to other control signals, to generate engine control commands. These commands reduce the steady-state drift of the vehicle trajectory and minimize the bending moments on the vehicle structure by reducing the angle-of-attack and lateral components of thrust. The control accelerometers are used for 30 to 120 seconds after liftoff and are not required once the vehicle is free of the atmosphere.

Four control accelerometers are used on the Saturn IB vehicle, two in the instrument unit and two in the S-IB stage. The accelerometers are mounted directly to the vehicle structure. One accelerometer of each set is used to control the vehicle pitch axis while the other is used to control the vehicle yaw axis.

Conventional Design

The basic components of the conventional accelerometer are the base assembly which includes the sensor, four printed circuit board assemblies, a case assembly with cover, an electrical receptacle, and an elapsed time indicator.

The base assembly is a flat plate on which the sensor is carefully positioned. Before the sensor is installed on the base, it is equipped with a heat sensing thermistor and wrapped in a heater jacket assembly. All other electrical and electronic components are mounted on the printed circuit board assemblies.

PHYSICAL CHARACTERISTICS

Physical characteristics of the conventional accelerometer are given in Table 1.

ELECTRICAL CHARACTERISTICS

Electrical characteristics of the accelerometer are given in Table 2.

OPERATION

The accelerometer contains four circuits that perform signal producing functions and three circuits that generate and control ac and dc power. Figure 4 illustrates the block diagram of the conventional control accelerometer.

TABLE 1. PHYSICAL CHARACTERISTICS OF CONVENTIONAL CONTROL ACCELEROMETER

Acceleration Range	0 to ±10 m/sec^2 (±1.02078 g)
Dimensions:	
Length (less connector)	0.127 m (5.00 in.)
Width:	
Enclosure	0.085 m (3.35 in.)
Base	0.102 m (4.00 in.)
Height	0.092 m (3.62 in.)
Weight	1.8 kg (4 lb)
Electrical Connections	19-pin connector
Operating Temperature Range	200°K to 344°K (-73°C to 71°C)

TABLE 2. ELECTRICAL CHARACTERISTICS OF CONVENTIONAL CONTROL ACCELEROMETER

Power Requirements:	
Accelerometer:	
Voltage	28 ± 4 Vdc
Power	8.4 watts
Heater:	
Voltage	28 Vdc
Power	28 watts
Output Requirements:	
At 0 acceleration	0 Vdc (differential)
At 10 m/sec^2	± 10 Vdc (differential)
Voltage scale factor	1.0 Vdc/m/sec^2
Ripple	Less than 120 mV
Output impedance	Less than 150 ohms

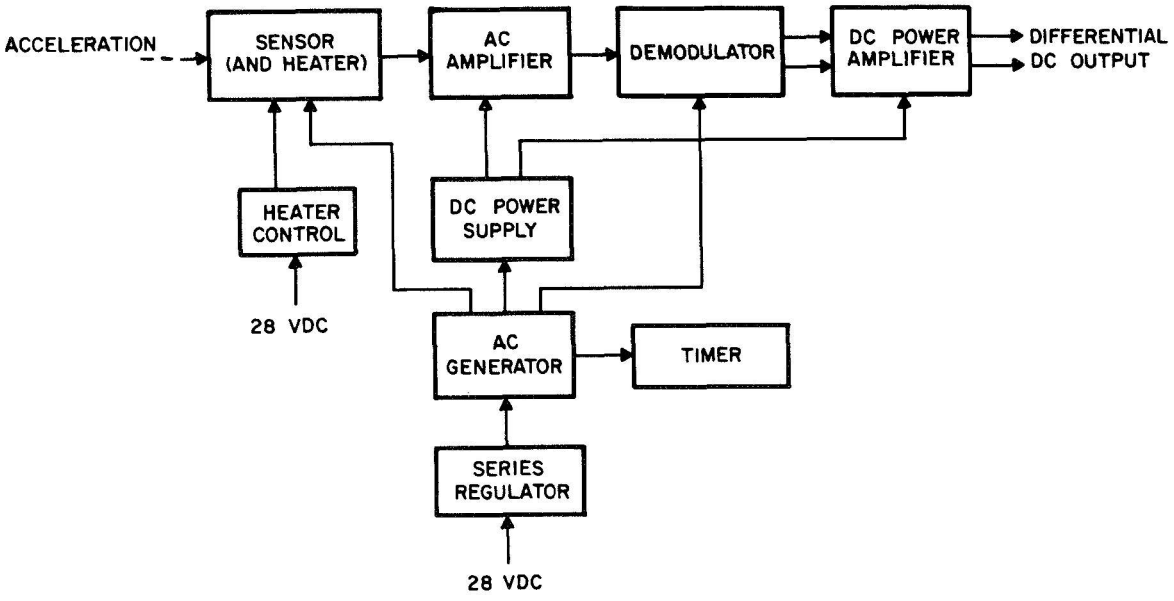


Figure 4. Block diagram of conventional control accelerometer.

The ac generator supplies the sensor with a 400 Hz voltage that excites the induction coils within the sensor. The sensor is designed so that a static condition does not produce an output voltage. A positive or negative acceleration, applied along the sensitive axis of the sensor, produces an ac output signal that can vary in both amplitude and phase angle. Signal amplitude is a function of the intensity of the applied acceleration, while the phase angle is determined by the direction in which the acceleration is applied. This signal is amplified by the ac amplifier and applied to the demodulator.

When the signal is rectified by the demodulator, the amplitude of the ac input signal determines the voltage differential between the two dc outputs, and the phase angle of the ac signal determines the relative polarity of the dc outputs. The dc output of the demodulator is filtered and amplified by the dc power amplifier. The dual output lines from the dc power amplifier have a differential output range of 0 to ±10 Vdc, representing an acceleration range of 0 to ±10 m/sec^2.

Power for the ac generator is supplied from an external 28-Vdc inverter through the series regulator. The series regulator maintains the voltage level to the ac generator between 19.5 and 20.5 Vdc. The 400-Hz output of the ac generator is rectified and regulated by the dc power supply, which provides the necessary bias voltages for the ac amplifier and dc power amplifier.

Microelectronic Design

The basic components of the microelectronic control accelerometer are the sensor assembly, seven flatpacks, two printed wiring interconnection boards, three small transformers, a transformer housing, an electrical receptacle attached to the sensor assembly, and a cover.

The sensor assembly is 0.082 m (3.3 in.) long by 0.044 m (1.75 in.) high by 0.041 m (1.62 in.) deep and contains the sensor. A 10-pin connector adapter, 0.024 m (0.95 in.) in diameter and 0.017 m (0.7 in.) in length, protrudes from the sensor assembly.

The seven flatpacks contain the power supply, oscillator, variable gain amplifier, fixed gain amplifier, demodulator, and discrete components that comprise parts of the power supply, amplifiers, and demodulator. The transformers are packaged in a separate housing and are stacked one on top of the other, then anchored with a nylon screw through the centers. The two printed-wiring interconnection boards sandwich the flatpacks and transformer housing.

PHYSICAL CHARACTERISTICS

Physical characteristics of the microelectronic accelerometer are given in Table 3.

TABLE 3. PHYSICAL CHARACTERISTICS OF MICROELECTRONIC CONTROL ACCELEROMETER

Accelerometer Range	0 to ±10 m/sec^2 (±1.02078 g)
Dimensions:	
Length	0.140 m (5.5 in.)
Width	0.041 m (1.62 in.)
Height (less connector)	0.044 m (1.75 in.)
Weight:	
Total assembly	500 g
Electronic assembly (less sensor and housing cover)	68 g
Electrical connections	10-pin connector
Operating temperature range:	
Sensor assembly	200°K to 344°K (-73°C to 71°C)
Electronic package assembly	218°K to 358°K (-55°C to 85°C)

ELECTRICAL CHARACTERISTICS

Electrical characteristics of the microelectronic accelerometer are given in Table 4.

OPERATION

Operation of the sensor of the microelectronic control accelerometer is the same as that of the conventional control accelerometer. The ac signal received from the sensor is amplified by the variable gain amplifier and applied to the demodulator. The amplitude of the ac input signal determines the dc output voltage and the phase angle of the ac signal determines the relative polarity of the dc output.

Power for the microelectronic control accelerometer is supplied by an external 28 Vdc source through a regulator that maintains the voltage level to the dc-to-dc converter between 19.8 and 20.2 Vdc. The dc-to-dc converter supplies 36 Vdc to the 2 kHz oscillator, fixed-gain amplifier, and variable-gain amplifier. Also, the dc-to-dc converter supplies a ±15 Vdc input to the demodulator. The output of the demodulator has a differential output range of 0 to ±10 Vdc, representing an acceleration range of 0 to ±10 m/sec^2. Figure 5 illustrates the block diagram of the microelectronic control accelerometer.

MICROELECTRONIC FABRICATION

Design Criteria

Preliminary design specifications limited the overall length of the control accelerometer to 14 cm (5.5 in.), with the height and depth of the electronic package the same as the sensor assembly. The acceleration range of ±10 m/sec^2 and the operating temperature range of 218°K to 358°K (-55°C to 85°C) was previously established. Four external electrical connections were required for the electronic package; 28 Vdc, 28 Vdc return, and two output connections.

Five individual circuit schematics were included in the total package. These were:

1. Power supply, including the regulator and the dc-to-dc converter
2. Oscillator
3. Fixed gain amplifier
4. Variable gain amplifier
5. Demodulator

A worst case ECAP computer program was written for each circuit to determine the tolerance of the electronic components. This program enables a higher yield of circuits by reducing the total number of resistors to be trimmed and increases the reliability by permitting an accurate selection of discrete components.

The planar layout of each circuit and the total package concept was conceived by the Hybrid Microelectronic Research Section. It was determined that the individual circuits would be packaged in 2.54-cm (1-in.) square flatpacks, with the leads from the flatpacks interconnected to the printed wiring boards by parallel-gap welding techniques.

TABLE 4. ELECTRICAL CHARACTERISTICS OF MICROELECTRONIC CONTROL ACCELEROMETER

Power Requirements:	
Accelerometer:	
Voltage	22 to 32 Vdc
Power	2.5 watts
Output Requirements:	
At 0 acceleration	0 Vdc (differential)
At 10 m/sec^2	±10 Vdc (differential)
Voltage scale factor	1 Vdc/m/sec^2
Ripple	Less than 100 mV
Output impedance	Less than 150 ohms

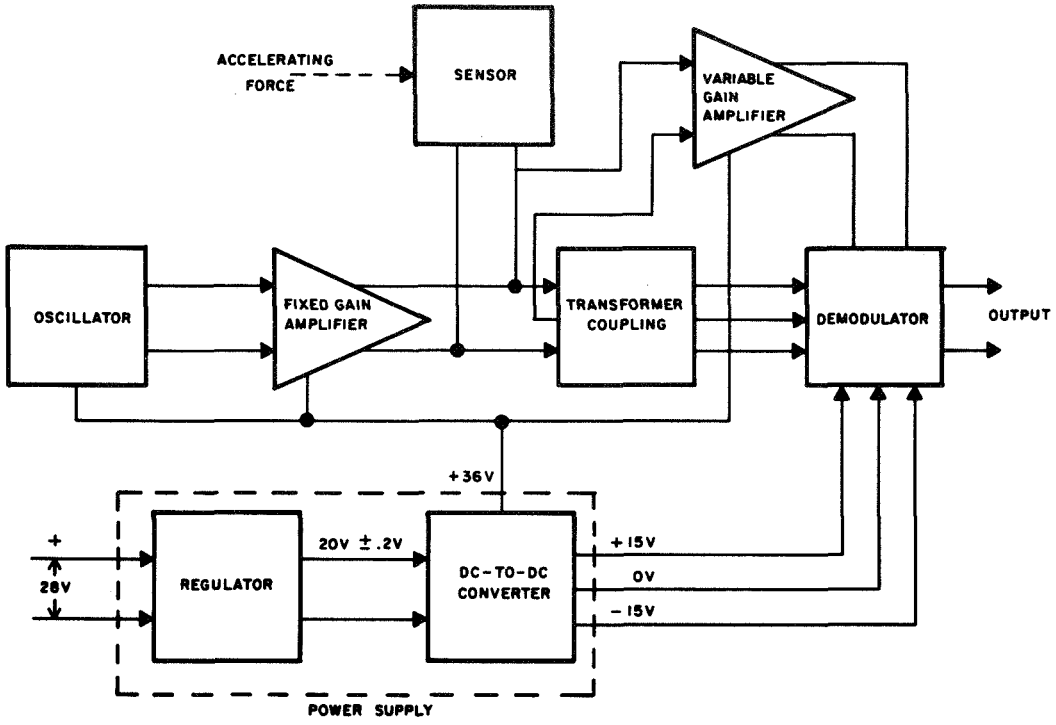


Figure 5. Block diagram of microelectronic control accelerometer.

The transformers contained in the individual circuits would be packaged in a separate housing with the leads soldered to the printed wiring boards. The circuits inside the flatpacks were to be assembled with no solders, eutectics, or conductive epoxies. All discrete components were to be attached to the substrate with epoxy.

Fabrication of Film Elements

EQUIPMENT

Each circuit was comprised of a combination of thin- and thick-film elements. Thick-film conductors were fabricated using a screen-printer and a batch furnace. The thin-film elements were fabricated using vacuum deposition equipment.

Once the thin-film resistors were deposited, trimming was accomplished using a laser trimmer.

MATERIALS

The conductor patterns and weld-pad areas were fabricated using a silver preparation. This compound is a metallo-organic paste and, when fired at high temperatures, the organic materials are driven off and only the metallic materials and glass binders remain. Each of the circuits contained both thin-film resistors and thin-film conductors. The thin-film conductors were vapor-deposited aluminum and were used exclusively as trim pads for definition of thin-film resistors. All thin-film resistors were vapor deposited nichrome. These resistors were deposited to a resistivity of 250 ohms/square. Silicon monoxide was deposited over all thin-film resistors for protective coating.

PROCESS

The first major step in the process of fabricating the film elements of the circuits was the

screen-printing of a conductor pattern on a substrate, using a metallo-organic compound in a paste form. After the paste is applied, it is allowed to dry and the substrate is fired until the organic materials are driven off and only the metal and glass binders remain. This screen-printed pattern must be electrically conductive and must form a durable base for attachment of discrete components and microwelding of external and component lead wires. The screens used were 325 stainless steel mesh and the substrates were fired at a temperature of 894°K (1150°F).

The next major step in fabricating the thin-film circuits is the deposition of the thin-film elements onto the substrate. The additive deposition process was used. This process is accomplished by depositing source material through metal masks in a vacuum of 13×10^{-4} N/m^2 (10^{-5} torr). Source, substrate, and mask positions can be changed within the vacuum system. Thus, all of the thin-film elements can be deposited in one pump-down cycle. This includes the conductor trim pattern, the thin-film resistors, and the dielectric passivation. By applying the dielectric passivation in the initial pump-down cycle and using laser trimming techniques, a higher circuit yield is attained. This process minimizes the resistance change of the thin-film resistors caused by oxidation from exposure to the atmosphere.

It is estimated that about 15% of the thin-film resistors in the control accelerometer required laser trimming. Laser trimming is accomplished by pulsing a laser beam on the edge of the resistor. When the laser beam strikes the resistor, the nichrome is evaporated and the resistor value increases. The laser beam is stepped along the resistor line until the desired resistor value is attained. Two advantages of laser trimming are:

1. The resistor material is totally evaporated and no particles are left on the substrate.

2. The resistor can be trimmed after a protective coating of silicon monoxide has been applied.

Figure 6 illustrates the laser trimming process.

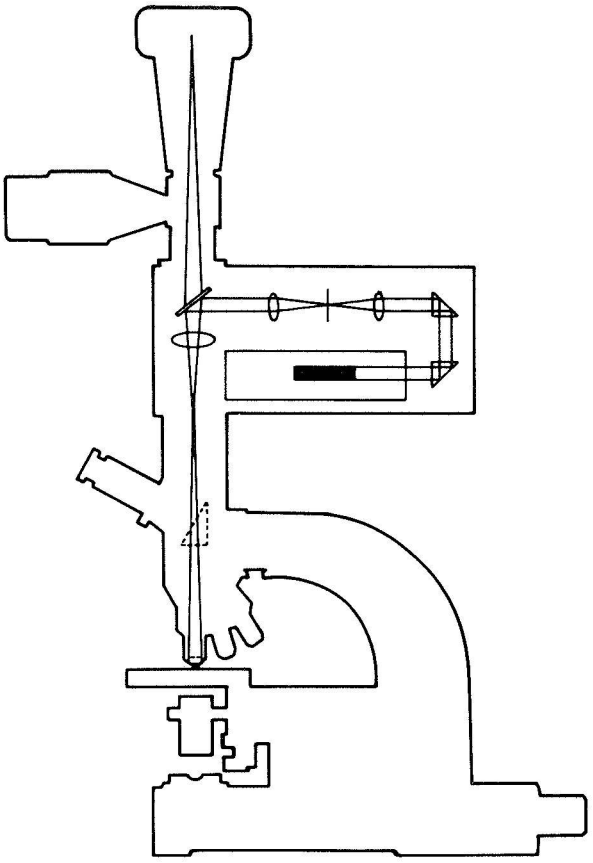


Figure 6. Laser trimming process.

Discrete Components

Discrete components were used for all semiconductors, capacitors, and low value resistors. The semiconductors consisted of Kotab and LID devices. The capacitors consisted of K1200 $BaTiO_3$ ceramic chips and solid tantalum chips while the discrete resistors were cermet pellets. Figure 7 illustrates the various types of discrete components used in the microelectronic control accelerometer.

BURN-IN

Every discrete component was burned-in for a period of 240 hours prior to assembly.

The transistors were burned-in with 100 mW power load at 298°K (25°C). This was accomplished by loading the transistors as shown in Figure 8. The base and collector supply voltages are adjusted such that the product of V_{CE} and I_E equaled 100 mW. The h_{fe} and h_{oe} characteristics of each

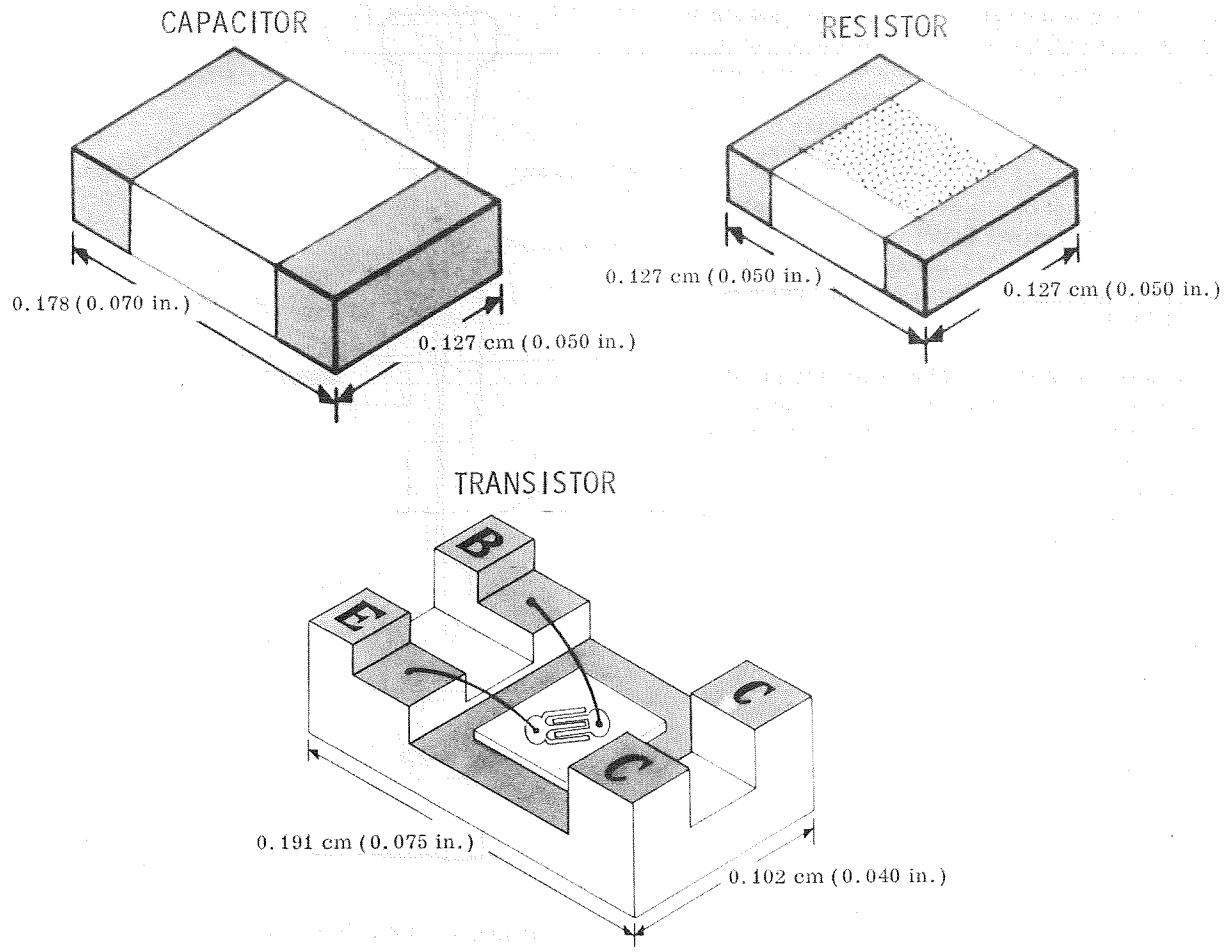


Figure 7. Discrete components.

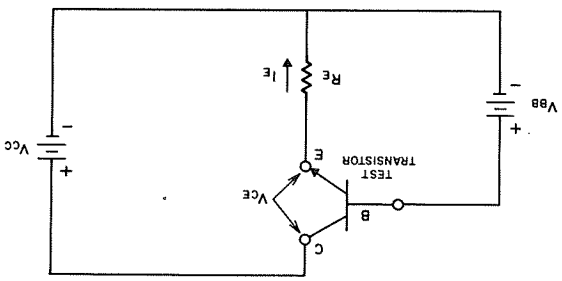


Figure 8. Burn-in test circuit for transistors.

transistor were photographed and recorded before and after burn-in. These photographs were retained for future reference.

Zener diodes were also burned-in at 100 mW power load and 298°K (25°C). The supply voltage is adjusted such that the product of the zener current and the zener reference voltage equals 100 mW. The burn-in test circuit for zener diodes is illustrated in Figure 9. The rectifier diodes were burned-in at a temperature of 398°K (125°C) under a no-load condition.

The ceramic capacitors were burned-in for a period of 240 hours at 398°K (125°C) with the rated voltage applied. The tantalum capacitors were burned-in at 358°K (85°C) with the rated voltage applied for a period of 240 hours.

The resistors were burned-in at 398°K (125°C) and 100 mW power load as determined from the

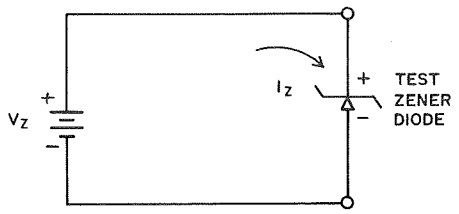


Figure 9. Burn-in test circuit for zener diodes.

formula $P = V^2/R$ where P is the power, V is the applied voltage, and R is the resistance value.

SELECTIVE MATCHING

The logging of burn-in test parameters permitted the selective matching of each component to its surrounding components in the circuit. Before the discrete components were assembled into microcircuit parts kits, the parameters of each component were reviewed and it was determined which individual component would best perform the required circuit function. This process reduced the number of trimming operations and assured traceability of each circuit element.

Attachment of Discrete Components to Substrate

Each of the discrete components was attached to the substrate with epoxy. There were two restrictions in the placement of components; (1) no components were allowed to bridge two conductive film elements such that an electro-potential difference could set up an electrolytic action within the epoxy and (2) no components were placed on resistor film elements.

Bonding of Component and External Leads

Bonding of component and external leads was accomplished using the parallel-gap bonding technique.

MATERIALS

With one exception, all of the component and external leads were 0.003 cm (0.001 in.) or 0.005 cm (0.002 in.) diameter gold wire. The tantalum chip capacitors had 0.008 by 0.030 cm (0.003 by 0.012 in.) gold-plated kovar leads. These ribbon leads were cut approximately 0.038 cm (0.015 in.) from the capacitor body and a 0.005 cm (0.002 in.) diameter gold wire was welded from the kovar ribbon to the substrate.

PROCESS

The parallel-gap bonding process is essentially a resistance heated thermo-compression bond. When the electrodes are contacted to the lead wire, a low resistance path is created and a dc square wave pulse at a constant voltage is induced across the weldment. This induces a current that passes through the lead wire and permits diffusion of the lead wire and the weld pad material. Figure 10 illustrates the current path during the parallel-gap welding process.

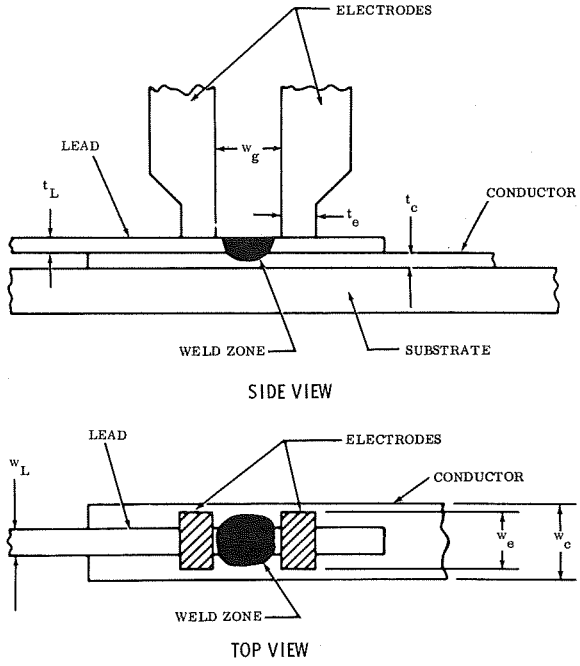


Figure 10. Parallel-gap welding process.

Attachment of Substrates to Flatpacks

The assembled substrate is attached to the flatpack with epoxy. This epoxy consists of a base material and a curing agent mixed in equal proportions.

Interconnection of Flatpacks

Interconnection of flatpacks was accomplished using the parallel-gap bonding technique.

EQUIPMENT

A special holding fixture was designed to hold the flatpacks between the two printed wiring boards during the process of placing the flatpack leads in the proper position.

MATERIALS

The flatpacks were 2.54-cm (1.0-in.) square kovar-ceramic packages with 0.013 by 0.038 cm (0.005 by 0.015 in.) gold-plated kovar ribbon leads. The printed wiring boards were a glass epoxy G-11 material with a nickel-plated copper clad conductor. The transformer housing was constructed of aluminum.

PROCESS

The flatpack leads were threaded into the printed-wiring boards by hand and these leads were parallel-gap bonded to the printed wiring boards in the same manner as previously discussed. The transformer leads and two external test-select resistors were soldered to the printed-wiring boards.

ELECTRICAL TESTS

Pre-Package Assembly Testing

Before the microcircuits were interconnected, they were tested in the breadboard setup. Figure 11 illustrates the breadboard setup. This enables a plug-in-plug-out check and assures the compatibility of each of the microcircuits. Potentiometers were used to determine the values of the test-select resistors.

Once each of the circuits was checked out on the breadboard and tuned to give the desired outputs,

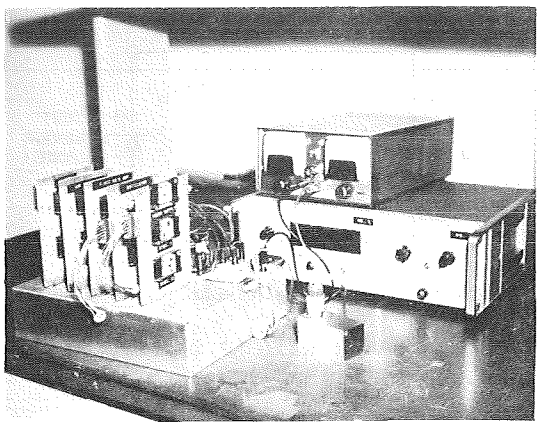


Figure 11. Breadboard test setup.

they were operated for a period of 240 hours under full load conditions before forwarding to the assembly lab. This test is to detect any incompatibility of the microcircuits.

Post-Package Assembly Testing

The complete accelerometer package was tested for dc output characteristics. The dc output is +10 volts when the sensor assembly is in the positive vertical position, -10 volts when the sensor is in the negative vertical position, and 0 volts when the sensor is in the lateral position. Two accelerometers have been fully packaged. One has completed nearly 1200 hours of bench testing under full load while the other has completed 800 hours. One of the accelerometers has completed 500 hours of continuous testing at 328°K (55°C). The microcircuits for two additional accelerometers have been completed and fully tuned and burned-in on the breadboard test setup.

CONCLUSIONS

The accelerometer system assembled was fully packaged within the design criteria and met all of the performance specifications. The packaging concept has proven feasible and no major modifications of the concept are recommended. However, the package concept is considered to be of the first generation and any further design would include the following: (1) elimination of thick-film conductor patterns in the power supply, demodulator, oscillator, fixed gain amplifier, and variable gain

amplifier, (2) changing the silver paste within the discrete packages to a gold paste, (3) inclusion of new discrete components such as beam lead transistors, LID's, ceramic chip capacitors, etc., (4) changing the conductor material of the printed wiring boards to gold-plated nickel, and (5) better heat sinking of the power supply flatpack and the components therein. Present state-of-the-art technology allows us to make all of these changes in a second generation accelerometer system.

AN MOS/LSI ANALOG-TO-DIGITAL CONVERTER

By

Owen Rowe, James J. Egan, and A. J. MacMillan

SUMMARY

The design and performance of a monolithic metal oxide semiconductor (MOS) analog-to-digital (A/D) converter are described. The converter accepts input voltages of ± 5 volts, has a 10-bit resolution including sign, operates at approximately 40 kHz, and utilizes MOS operational amplifiers.

INTRODUCTION

This paper describes the design of a monolithic analog-to-digital converter using p-channel enhancement mode technology. The converter, which utilizes a charge division method for digitizing, is composed of four basic functions; namely, a capacitance switching network, an integrating amplifier, a voltage comparator, and a digital control section. (See Figures 1 and 2.)

ANALOG-TO-DIGITAL CONVERTER

The operation of the converter is based upon the successive division of a charge proportional to the analog input between two equal (within the conversion accuracy) capacitors, and its subsequent integration with a charge proportional to a reference voltage. The polarity of an integrating amplifier output, after one half of each bit time of the conversion, is sensed

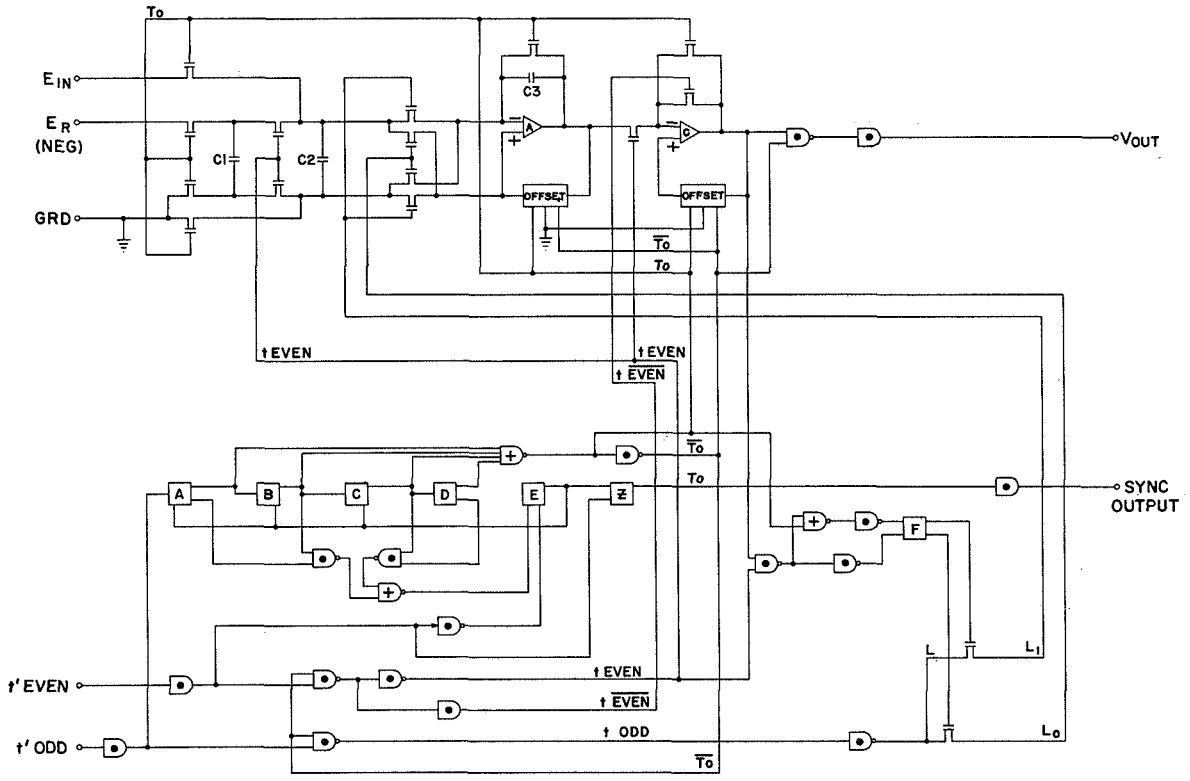


Figure 1. Analog-to-digital converter MOS/LSI.

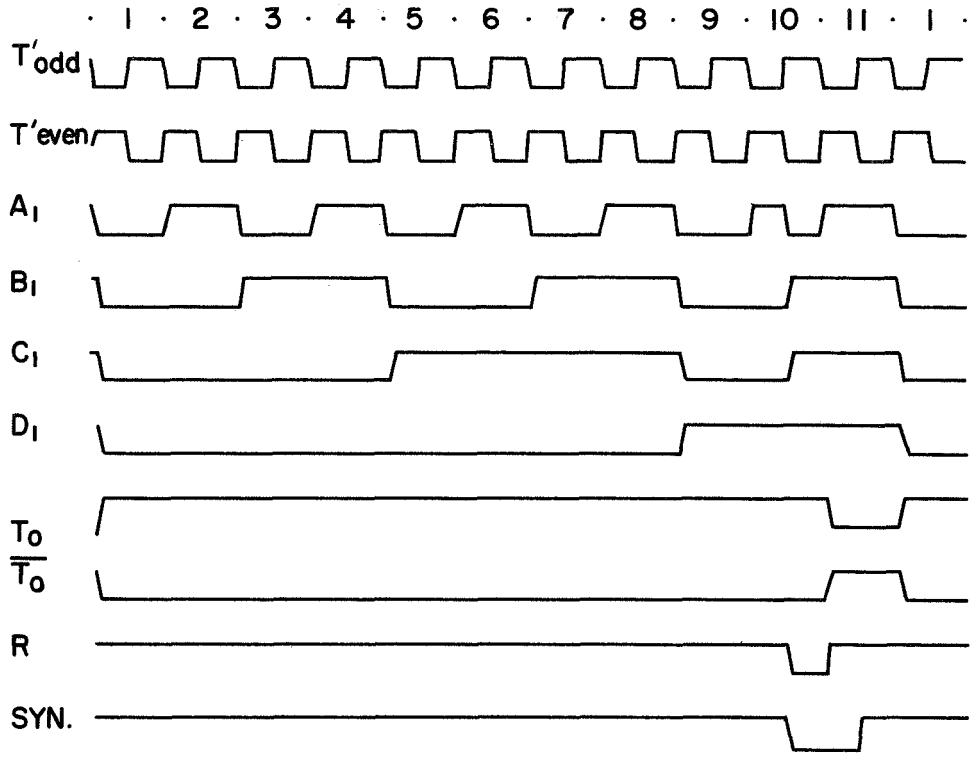


Figure 2. Analog-to-digital converter clock and control logic phasing.

by a voltage comparator and represents first the sign and subsequently the presence of a binary 1 or 0.

The MOS capacitors used in the capacitance switching network employ p-n junction isolation and are precisely balanced topologically and schematically to offset the effect of switching transients and parasitic capacitances.

A single operational amplifier configuration is used for both the integrating amplifier and voltage comparator functions. The amplifier design employs three successive differential stages and current mode feedback to minimize the effect of supply voltage and MOS device parameter variations on amplifier performance and operating point. Also, a dynamic offset and drift correction scheme is utilized wherein the amplifier is operated in a unity gain mode for one bit time between conversions. Its output is sampled, stored on a capacitor, and subsequently added to the amplifier input during normal operation so as to buck out any offset or drift voltage.

The control section of the converter divides and operates on a two-phase pulse input, whose frequency is eleven times the conversion rate, to produce the necessary timing and control signals used in the converter operation.

The design goals for the monolithic MOS analog-to-digital converter are as follows:

Resolution	10 bits including sign
Code	Binary using sign magnitude representation
Conversion Rate	40 000 per second
Range	±5.00 volts full scale
Output Logic Levels	0, -20 volts
Accuracy	0.05 percent ±1/2 LSB @ 298.15°K (25°C)
Stability	0.005 percent per 90 days
Temperature Coefficient	0.001 percent per 274.15°K (1°C) (worst case)

The converter will occupy a chip area of approximately 30.48×10^{-4} by 30.48×10^{-4} meter (120 by 120 mils). Supply voltage requirements are -27 volts and +12 volts, both ±1 percent, and +5.12 volts, ±0.1 percent. Power dissipation will be less than 200 milliwatts. Initial packaging plans call for the use of a round 0.953 cm (0.375 inch) diameter 22-lead flatpack that will allow for the availability of a number of internal test points in addition to the required pins.

COMPUTER-AIDED DESIGN OF MOS/LSI ARRAYS

By

Carl E. Winkler

It is assumed that Marshall Space Flight Center will become deeply involved in long duration missions such as the Space Shuttle and the Space Station. These efforts will require high reliability electronics if our systems are to perform satisfactorily under environmental stress over extended periods. A study by Moore-Peterson Associates for NASA Headquarters states that "substantially all of the major failure mechanisms can be traced to the interconnection problem." Granting that this is true, the way to reduce electronic failures is to cram more and more circuitry into a single monolithic silicon chip. As this idea is developed, large scale integration (LSI) results, and the application of the overall chip becomes less universal. The trend seems to be toward development of low volume custom circuits to achieve high reliability.

To facilitate acquiring low volume LSI arrays from integrated circuit manufacturers and to minimize the turnaround time from design to circuit test, computer-aided design (CAD) techniques are being applied. This will provide the MSFC design engineers with several options in procuring their circuits from industry. The interface between the design engineer and the integrated circuit manufacturer can be on any level from Boolean equations to final artwork for the fabrication masks. If the artwork option is chosen, as provided by in-house CAD facilities, the turnaround time and cost should be minimized.

At a CAD conference held at the Electronics Research Center in 1969, it was learned that the National Security Agency (NSA) had a collection of computer programs developed to lay out and analyze p-channel metal oxide semiconductor (MOS) arrays automatically. Copies of the tapes and documentation designed for operation on a GE 625 computer were obtained from NSA. However, since such a computer is not available at MSFC, the programs need to be converted for our use. This task is presently underway.

Figure 1 helps to show that the MOS technology lends itself well to automated techniques. This figure can be used to describe the sequence of steps required in the fabrication of a P-MOS transistor; however, it is not the intent of this paper to do this, but rather to point out the fact that only four masks and a single diffusion typify the fabrication process. On the other hand, the bipolar technology requires seven masks and two successive diffusions. It is then obvious that for the P-MOS process, if the diffusion time and temperature and the impurity flow are carefully controlled, the final device characteristics are governed by the planar geometry of the masks.

The transistor described in Figure 1 is called a p-channel enhancement mode device. This means that a p-region is created at the surface on the n-region immediately under the gate when a negative voltage of sufficient magnitude is applied to the gate. No conduction from source to drain is possible until a certain threshold voltage, typically -2 to -5 volts, is reached. With the source and substrate at ground, a negative voltage on the drain, and a sufficiently negative voltage on the gate to exceed threshold, conduction by hole flow takes place. Because of the threshold voltage requirement, a certain amount of noise immunity in digital applications exists in enhancement mode devices.

A further simplification afforded by the MOS technology stems from the fact that a transistor can replace a resistor. The geometry can be adjusted to achieve the desired resistance between source and drain, and a resistor made in this way only requires about one-thirtieth the silicon area that a diffused resistor would occupy. Furthermore, the MOS structure forms a natural parallel plate capacitor with the aluminum and silicon being the two plates and the silicon dioxide being the dielectric. Thus, only transistors need to be fabricated, since transistors can be used as resistors and capacitors. The packing density is further increased since direct coupling techniques are employed.

Figure 2 shows a basic inverter first with a load resistor and then with a transistor taking the place of this resistor. The load MOS would typically have a g_m (transconductance) of 10 while the inverter MOS would have a $g_m \approx 100$, where

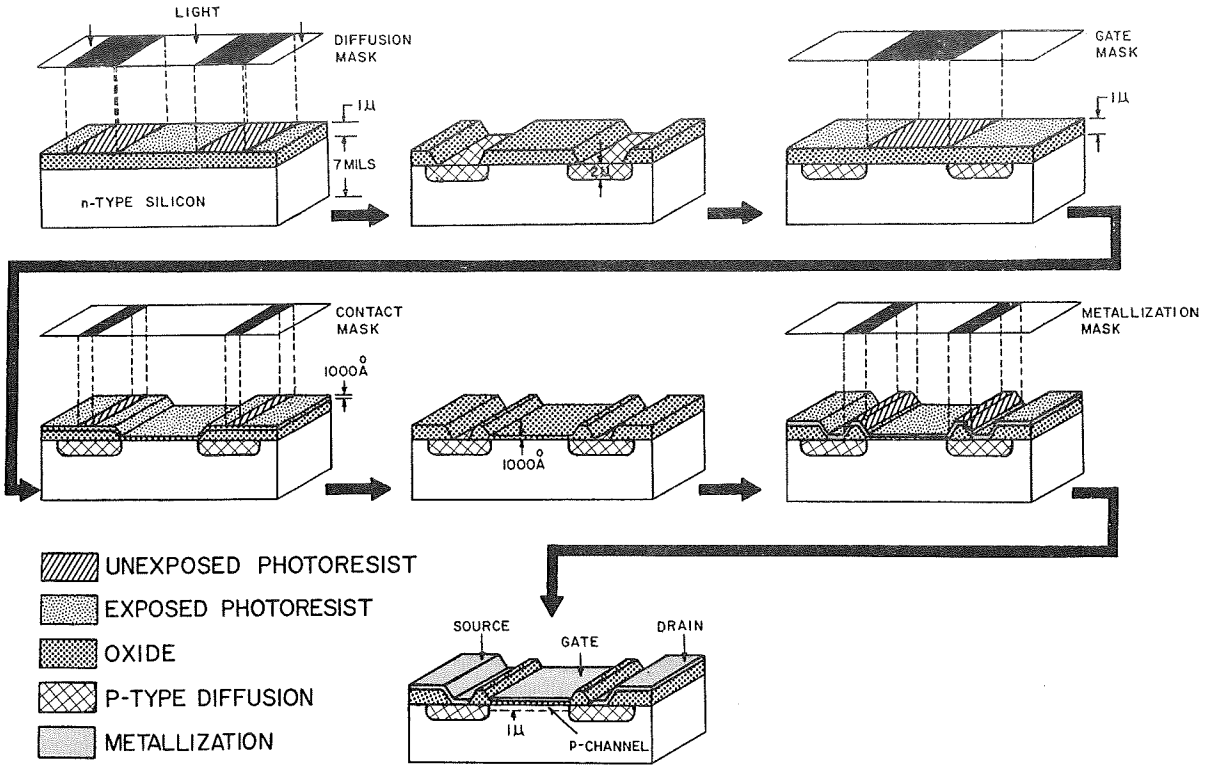


Figure 1. Fabrication of a p-channel MOS transistor.

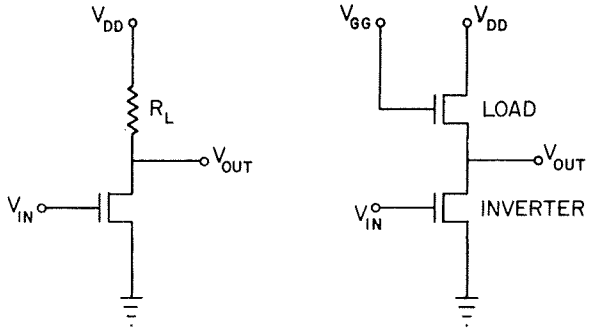


Figure 2. Basic inverter with a load resistor and with a transistor substituted for the resistor.

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}} ,$$

I_D is the drain current,

V_G is the gate voltage,

and

V_{DS} is the drain to source voltage.

The transconductance can be approximated by

$$g_m \approx \frac{40W}{\ell} ,$$

where

W is the width of the channel

and

ℓ is the length of the channel.

A second transistor connected in parallel with the inverter MOS of Figure 2 would result in a two-input NOR circuit. A second transistor connected in series would produce a two-input NAND circuit. This supposes that a negative voltage is counted as "1" while ground is counted as "0."

Figure 3 introduces the two-phase clocking scheme and demonstrates the bilateral properties of MOS devices in the charging and discharging of capacitors. MOS transistors used in this way between stages are called transmission gates. The circuit can be traced through in the following way. Suppose a "1" (negative voltage) appears at the input on the left. This turns the input transistor on; and during the duration of ϕ_1 when the first transmission gate is on, a "0" becomes stored on the MOS capacitor (shown dashed), since ground is effectively connected to its gate. Now ϕ_1 goes to ground and a "1" appears at the output when ϕ_2 becomes negative, resulting in the one-bit delay shown.

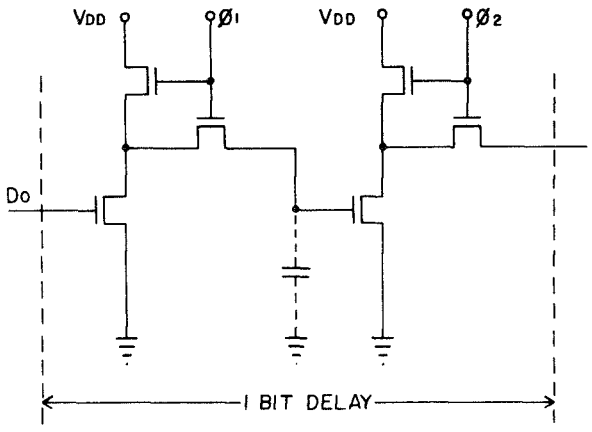


Figure 3. Shift register technique.

The basic logic that has been indicated combined with the two-phase clock can be extended to perform very complex logic functions. Three types of MOS arrays can be identified and compared; i.e., custom-designed, universal, and standard cell. These will be discussed briefly in turn.

Custom-designed arrays require a precision draftsman making unique layouts for all masks. This is tedious, costly, and very time consuming. It typically takes several months to produce error-free artwork. A good layout man can minimize the required silicon area, however. This maximizes the fabrication yield, and if the projected volume is high enough, it is probably worth considering.

Another approach to custom LSI is the universal array approach. Several often-used functions such as NOR gates and flip-flops are built into a fixed pattern, but the components are not interconnected; that is, the first three masks are fixed and the devices can be processed through three levels of masking and then stored. The final wiring mask is customized. This approach features a short turn-around time; however, yield suffers because of inefficient use of silicon area. Interconnection crossovers present some problems also.

The standard cell approach to LSI is based on a computer inventory of basic circuits and makes maximum use of automation. The height of each cell is constant; however, the silicon area is minimized to produce good yield by minimizing cell width. This concept features a fixed bus structure and standardized input and output locations. The information for the layout of masks is stored in a computer, and the time lapse from design to artwork generation is very short. The computer handles the details on remembering how each cell is constructed, arranges them efficiently, and generates the artwork for a mask set. The masks are stepped to produce identical patterns all over the silicon wafer. This approach to LSI requires a good grasp of a very complex set of computer software.

The system of programs obtained from NSA constitutes the standard cell approach. It contains a library of about 130 standard cells and 5 major programs:

- Placement Route Fold (PRF)
- Artwork Generation
- MOS Logic Block Simulator
- Signal Trace
- Transient Analysis

The first two programs are used to translate a logic design into precision artwork for use in device fabrication. In practice, the first program to be used is the MOS logic block simulator. This simulates the logic systems of interconnected standard cells. The program is driven from punched cards that describe the cell types and the interconnection network. The idea is to check and correct any logic errors before proceeding to PRF. It has been estimated that for complex logic designs there are about three chances out of four that some logic error exists; therefore, this simulation program is very important.

The PRF program is responsible for final cell placement on the chips. Standard cells, all of the same geometrical height but varying in width according to complexity, are arranged in a straight line layout by the computer, with interconnection length and crossovers being minimized. Crossovers are provided for by crossing metal lines over diffused p-regions with an insulating layer of silicon dioxide between them. Finally, the straight line layout is folded to give a somewhat square configuration.

Once the layout is set, the Artwork Generation Program generates light aperture and motion commands that control a Gerber Plotter. The four required sets of artwork are plotted out at 100 × the final size, reduced, and stepped to produce the fabrication masks.

The Signal Trace Program is designed to run as a subroutine to the PRF program and provides a highly accurate time analysis prediction for the desired array. The Transient Analysis Program is used to evaluate the response time of the basic standard cells.

Figures 4 and 5 are copies of pages as they appear in the standard cell library notebook that the designer has at his disposal. The following information is given in Figure 4: cell name, pattern number, schematic, logic diagram, truth table, logic equations, terminal capacitance, and date of design. NSA periodically distributes notebook additions and updates, and these are used to update the computer standard cell library. Figure 5 is a composite cell layout. The four levels of masks can be retrieved from this figure. The ϕ_1 version is on the left and the ϕ_2 version is on the right. Solid lines outline the areas for making p-diffusions, either for source or drain or for providing a crossunder; metal areas are dashed. The first-contact hole and gate oxide-removal mask can be seen crosshatched from upper right to lower left. The areas crosshatched from upper left to lower right are the second-contact hole mask.

The bus structure for the supply voltage, two-phase clock, and ground can be seen along the top of the cell in Figure 5 while the input and output pads are along the bottom. All standard cells are 27.69×10^{-5} meter (10.9 mils) in height. The layout of such cells is digitized, and four orientations on any cell are available. The layout can be flipped left to right or top to bottom.

Figure 6 demonstrates the folded configuration. The various busses can be identified. The widest bus is the V_{DD} supply voltage and then come the ϕ_1, ϕ_2, and ground busses. The chip is about 22.86×10^{-4} meter (90 mils) on a side and includes the pads for connection to the package leads.

In order to become operational with the programs outlined here, the services of M&S Computing Company, a Huntsville firm, have been contracted to implement Artwork Generation and PRF on a computer presently located in Astrionics Laboratory. This requires a conversion from magnetic tape to paper tape to satisfy the Gerber Plotter. The contractor will then conduct training sessions in the use of the software package. Later the other three programs will be implemented.

Concurrent with this contractual effort is the in-house fabrication of standard cells. Several types of cells have been made and tested. Simple counters and shift registers have been built up. The plan is to furnish the design engineers with in-house fabricated cells along with data sheets so that they can proceed with a breadboarding and familiarization phase.

Since this standard cell approach is based on the two-phase logic scheme to achieve higher frequency operation and lower power, training in two-phase logic design as well as four-phase, static, and complementary is planned for the near future for systems design engineers.

The advantages of standard cell design automation are numerous. Improved accuracy results from the elimination of manual drafting with inherent human errors. Each cell is accurately digitized according to various layout rules, check plotted, and committed to the library magnetic tape storage. Subsequent use of a given cell is, therefore, free of human error. Final artwork can be available in several days instead of a few months. The Signal Trace Program utilizes the capacitance loading figures furnished by the PRF program to give a pictorial printout of each network of logic including the time response of each node. Accurate logic simulation as provided for by the MOS Logic Block Simulator Program allows the user to check and correct his logic before proceeding to PRF. Because a given cell is designed only once, the engineer can afford to spend much more time optimizing the electrical characteristics before insertion into the library.

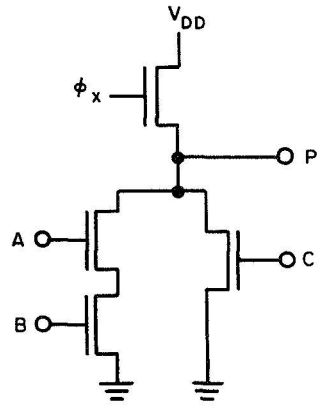
BANNING THICK OXIDE STANDARD CELL

THREE INPUT AND NOR, 2pF

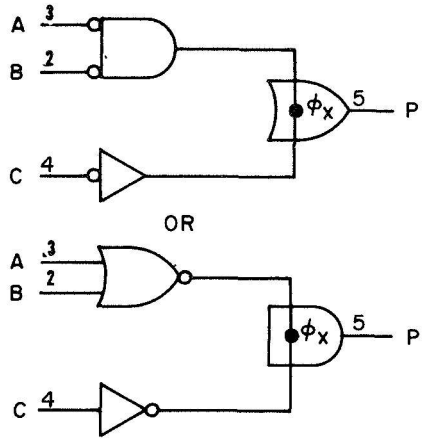
PATTERN NO. 2230 (ϕ_1)
2240 (ϕ_2)

APRIL 1968

SCHEMATIC



LOGIC SYMBOL



TRUTH TABLE

A	B	C	ϕ_x	P
0	*	0	0	P_{t-1}
*	0	0	0	P_{t-1}
*	*	1	*	0
1	1	*	*	0
0	*	0	1	1
*	0	0	1	1

*MEANS EITHER STATE

LOGIC EQUATIONS

$$P = (P_{t-1}) \cdot (\overline{A \cdot B + C}) \cdot \overline{\phi_x} + (\overline{A \cdot B + C}) \cdot \phi_x$$

$$= (P_{t-1}) \cdot (\overline{A} + \overline{B}) \cdot \overline{C} \cdot \overline{\phi_x} + (\overline{A} + \overline{B}) \cdot \overline{C} \cdot \phi_x$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF	
C_A	3	470	470
C_B	2	475	475
C_C	4	275	275
C_P	5	335	315
PATTERN NO.		2230	2240

THREE INPUT AND NOR • 2230/2240 • APRIL 1968

DS-15

Figure 4. Copy of page from standard cell library notebook.

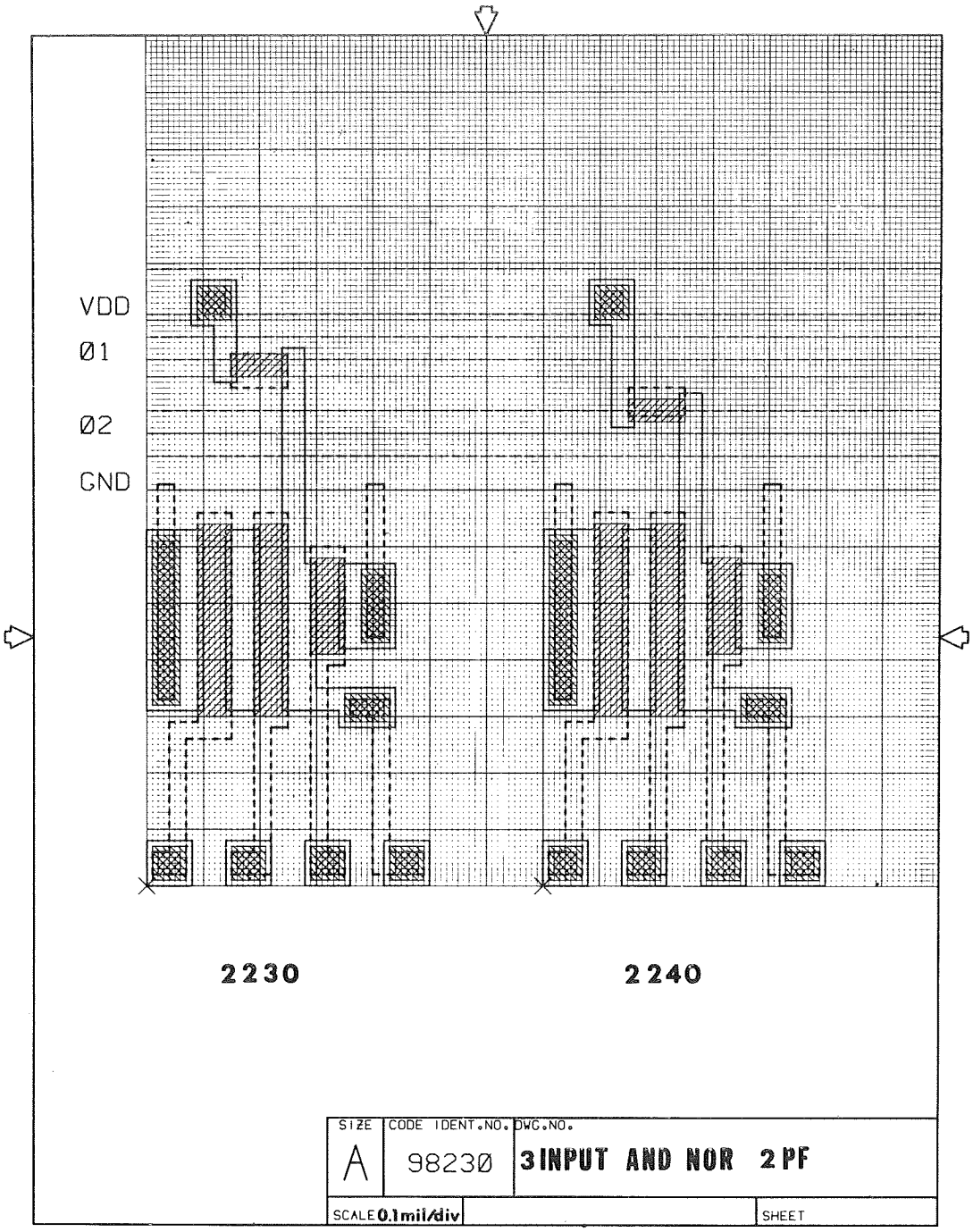


Figure 5. Copy of page from standard cell library notebook.

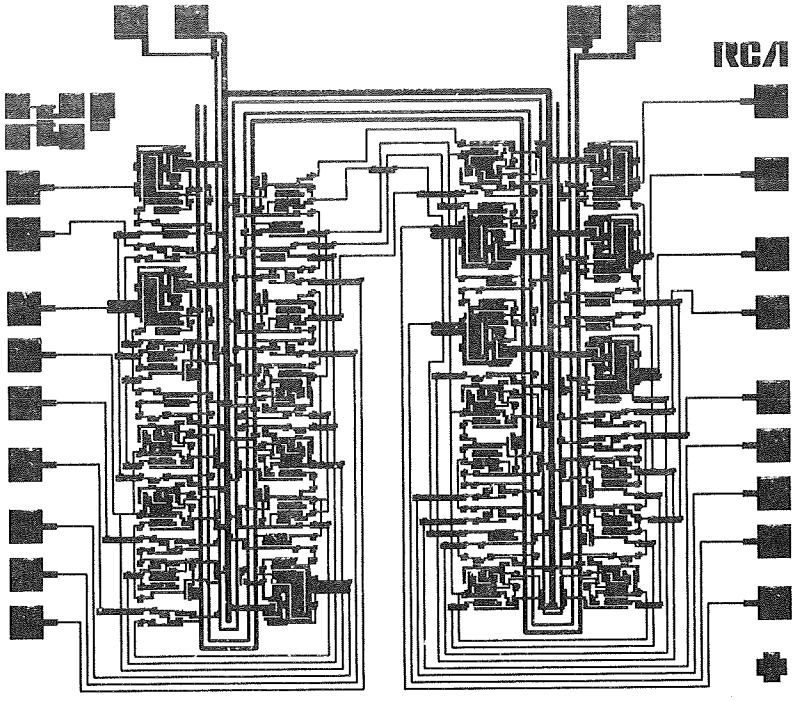


Figure 6. Demonstration of the folded configuration.

Several integrated circuit manufacturers are employing the standard cell approach to LSI and many are using the same library that is available at MSFC. Obviously, the realization of an operational standard cell capability will be extremely advantageous to the MSFC systems design engineers when dealing with those companies that will be supplying LSI arrays for the Space Shuttle and Space Station.

ADVANCED AEROSPACE COMPUTER TECHNOLOGY

By

Harrison Garett*

LIST OF ABBREVIATIONS

Abbreviation	Meaning
SUMC	Space Ultrareliable Modular Computers
LSI	Large Scale Integration
ROM	Read Only Memory
Chip	A slice of silicon on which the C-MOS devices are made
ER	Exponent Register
PRR	Product Remainder Register
PRRG	Product Remainder Register Gated
MARG	Memory Address Register Gated
IR	Instruction Register
MQR	Multiply Quotient Register
MAR	Memory Address Register
FPM	Floating Point Multiplexer
PRM	Product Remainder Multiplexer
MAM	Memory Address Multiplexer
MQM	Multiply Quotient Multiplexer
MUX	Multiplexer
EALU	Exponent Arithmetic Logic Unit
ALU	Arithmetic Logic Unit
SCU	Sequencing Control Unit
SPM	Scratch Pad Memory
FCU	Function Control Unit
TLU	Timing and Logic Unit
DEX	Derived Exponent
MOS	Metal Oxide Semiconductor
C-MOS	Complementary Metal Oxide Semiconductor
P-MOS	P-Channel Metal Oxide Semiconductor
TTL	Transistor Transistor Logic

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* The architecture, system design, and logic design of the Space Ultrareliable Modular Computers were performed by Mr. R. C. Asquith of the Advanced Computer Office, Computers Division, Astrionics Laboratory, Marshall Space Flight Center. Mr. Asquith has been engaged in research and development of flight computers throughout his employment with NASA. His dedicated and ingenious efforts on the SUMC have greatly advanced the state-of-the art in aerospace computers. The writer would like to thank Mr. Asquith for his assistance in the preparation of this paper.

INTRODUCTION

This paper describes the work being performed in-house at Marshall Space Flight Center by the Computers Division of Astrionics Laboratory on the design and development of a "family" of advanced aerospace computers called the Space Ultrareliable Modular Computers (SUMC). The computer development is being directed toward application on space missions in the 1975 to 1980 time frame. The SUMC advances the technology in computer design and logic implementation, and will employ the latest technology in memory and power supply design. The unique functional features designed into the SUMC result in a high degree of flexibility; i.e., variable and sophisticated instruction set, modular word length, and the availability of numerous registers for arithmetic operations. Standardization has been designed into the SUMC, and only eight different types of large scale integrated (LSI) chips are required to implement any one of the total family of advanced aerospace computers. This feature results in a lower manufacturing cost and it affords some reliability enhancement.

The SUMC can be applied across the entire spectrum, from a microprocessor to a full multiprocessor, by merely selecting the capability required for a particular application.

SCOPE

SUMC Architecture and Characteristics

The architecture of the Space Ultrareliable Modular Computers is described below. The computers have been organized as shown in Figure 1. The computers are microprogrammed via a read only memory (ROM) that provides the capability for a variable instruction set. A high degree of modularity has been designed into the SUMC. The word length is expandable in 4-bit bytes from 16-bits to any desired word length. The basic SUMC is a 32-bit machine with floating point. The computer has been partitioned in 4-bit slices, with each 4-bit slice contained on three LSI chips. A total of eight types of LSI chips is required to implement the entire family of SUMC. The LSI chip types and quantities required for various computers within the SUMC family are shown in Table 1, and a brief description of each type of LSI chip follows.

ARITHMETIC LOGIC UNIT (ALU)

The logic contained on the ALU is shown in Figure 2. The unit has the capability to perform the following: add, subtract, reverse subtract, and logical functions (AND, OR XOR, 1's and 2's COMPLEMENT). When interfaced with external circuitry, the capability exists to perform the following: 4-bit multiply, 2-bit divide, 2-bit square root, right shifts, and left shifts.

MULTIPLEXER REGISTER UNIT (MRU)

The MRU contains three multiplexers and four registers. The functions performed by this unit in the system are to provide temporary storage of data and to gate and shift data as required.

SCRATCH PAD MEMORY (SPM)

The SPM provides temporary storage, program addressable registers, program counter, etc.

FLOATING POINT MULTIPLEXER UNIT (FPMU)

The FPMU contains the necessary logic to provide floating point capability.

SEQUENCE CONTROL UNIT (SCU)

The SCU provides the address capability for the ROM.

READ ONLY MEMORY (ROM)

The ROM provides the necessary storage to implement the instruction set. Presently this storage has been sized at 512 words, 72 bits.

FUNCTION CONTROL UNIT (FCU)

The FCU contains the logic associated with MPY, DIV, and SQUARE ROOT. It also contains some storage registers and control lines.

TIMING AND LOGIC UNIT (TLU)

The TLU contains logic associated with error detection and data control.

The SUMC functional characteristics, for a 32-bit machine, are shown in Table 2.

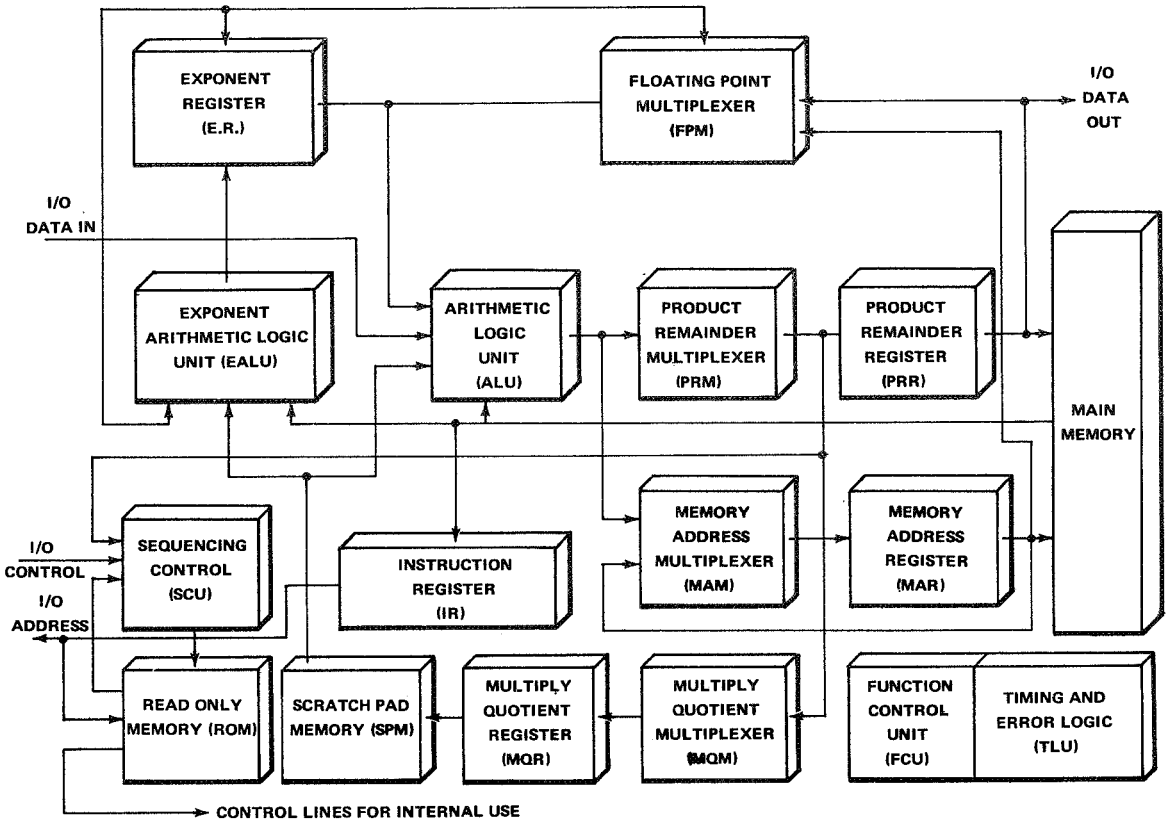

Figure 1. Space Ultrareliable Modular Computer (SUMC).

TABLE 1. LSI CHIP TYPES AND QUANTITIES REQUIRED FOR VARIOUS COMPUTERS WITHIN THE SUMC FAMILY

LSI Chip Type	Quantity of LSI Chips Used		
	16-Bit	24-Bit	32-Bit Floating Point
Arithmetic Logic Unit	5	7	11
Multiplexer Register Unit	4	6	9
Scratch Pad Memory	4	6	8
Floating Point Mux	0	0	4
Sequence Control Unit	1	1	1
Read Only Memory	12	12	14
Function Control Unit	2	2	2
Timing and Logic Unit	2	2	2
Total	30	36	51

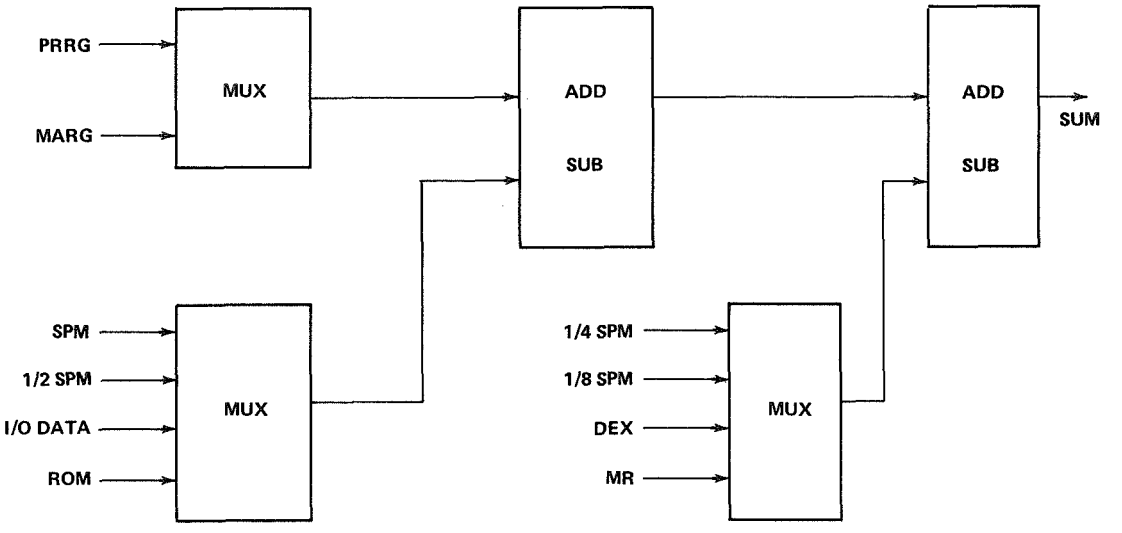

Figure 2. Arithmetic and logic unit functional diagram.

TABLE 2. SUMC 32-BIT FUNCTIONAL CHARACTERISTICS

Arithmetic Features

Registers: 16 accumulators
4 to 16 index registers
4 to 16 base registers
or 16 general purpose registers

Type: Parallel

Number Installed: 256 (variable)

Word Formats: ≈4 μsec

Multiplication Time: ≈ 11 μsec

Divide Time: ≈ 17 μsec

Floating Point Addition: ≈ 5 to 7 μsec

Floating Point Multiplication: ≈ 13 μsec

Addressing

Address: All memory directly addressed

Absolute address is the displacement + index + base

Input/Output

Defined by Application: Interrupts, number channels, word rate, etc.

Scratch Pad Memory

Use: Temporary storage, base, program counter, accumulator, and index registers

Word Length: 32 bits

Cycle Time: 1 μsec

Capacity: 64 words

Type: Semiconductor

Main Memory

Word Length: 32 bits

Cycle Time: 1 μsec

Capacity: Up to 4 billion words addressable

Type: Being studied; core, film, plated wire, other

Special Features

1. Modular construction expandable word size; in 4-bit bytes (eight chip types)
2. Microprogrammed: variable instruction set
3. Flexible data addressing

SUMC Technology

The SUMC design is being implemented utilizing LSI complementary metal oxide semiconductor (C-MOS) technology. The C-MOS technology affords the best power-speed characteristics as compared to bipolar or p-channel metal oxide semiconductor technology (P-MOS). The degree of LSI being employed is on the order of 250 logical gates per silicon chip. This equates to approximately 1000 active devices per chip. The packaging approach being pursued is shown in Figure 3. There are basically four levels of assembly; i.e., LSI chip, substrate module, page assembly, and computer assembly. Each of these levels is briefly described below.

LSI CHIP

The LSI chips are presently sized to contain up to 1000 active devices with terminations "to" and "from" the chip achieved through the use of up to 80 beam leads. There are eight LSI chip types required. The total usage of each type depends on the particular SUMC being implemented as shown in Table 1.

SUBSTRATE MODULE

The substrate module is composed of a basic alumina substrate on which circuit patterns are applied either by thick- or thin-film techniques. A number of LSI chips (presently sized for six) are mounted to the substrate and, a protective cover is placed over the assembly. The substrate module has up to 160 leads to interface to the next higher assembly.

PAGE ASSEMBLY

There are a number of alternatives available when going from a substrate module level to the next higher level. These alternatives are application-dependent with determining factors such as cost, repair concept, etc. If, for example, the application required only a microprocessor with minimum repair capability, a SUMC could be configured as shown in Figure 4. If, however, it was required that the microprocessor have repair capability, a SUMC could be configured as shown in Figure 5. The primary approach being implemented in the SUMC 32-bit machine under development is as shown in

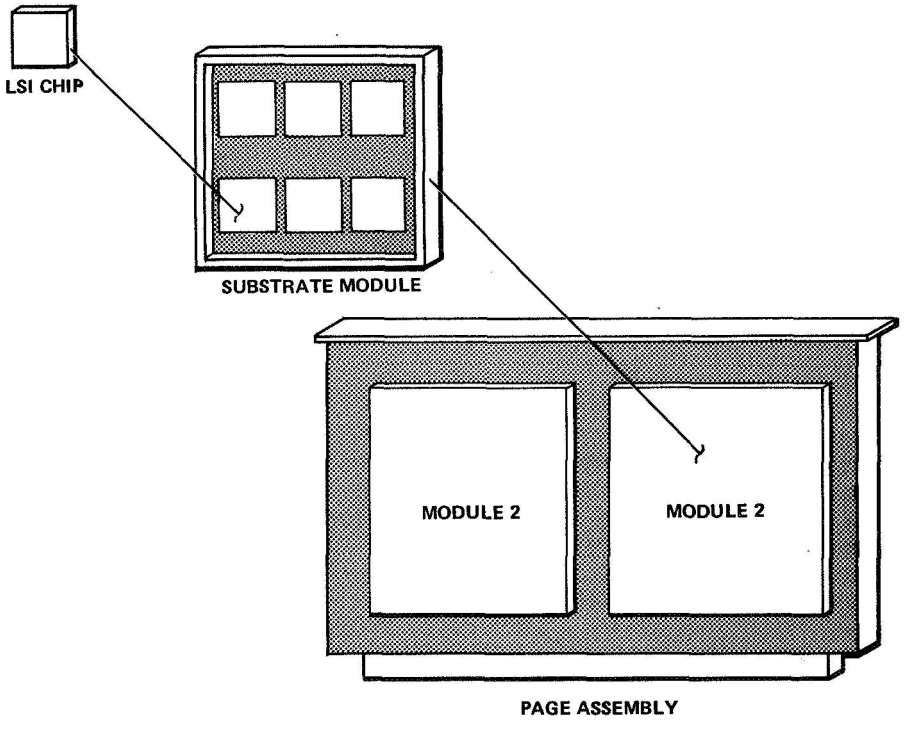

Figure 3. SUMC packaging technology.

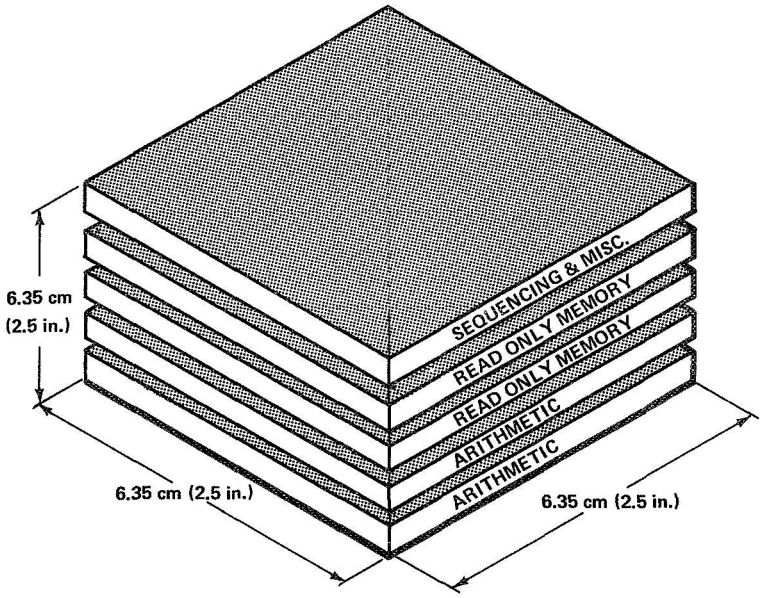

Figure 4. Microprocessor 16-bit SUMC.

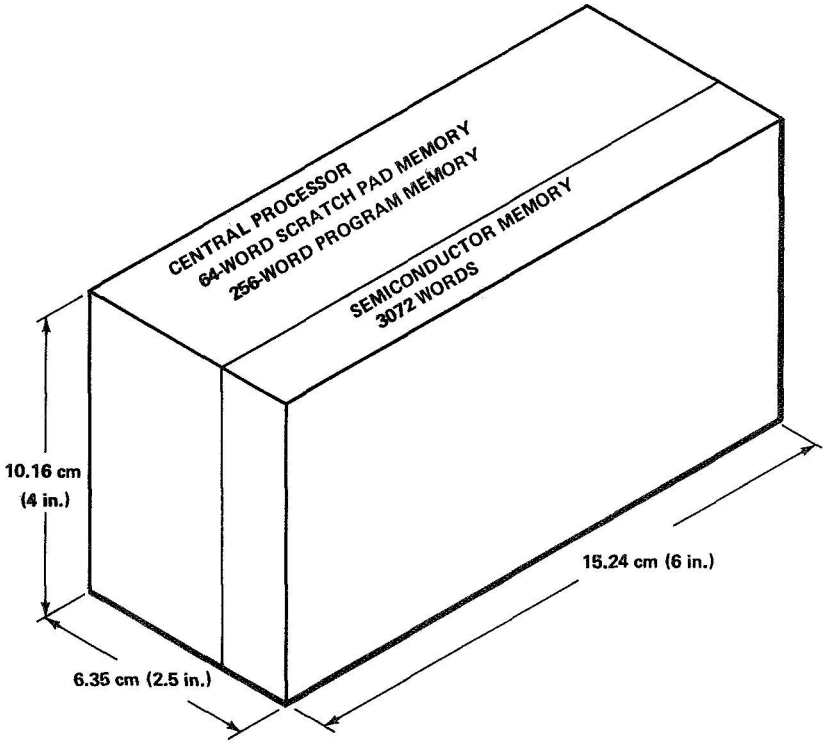

Figure 5. Microprocessor 16-bit SUMC.

Figure 3. The page assembly is made up of a page frame, two multilayer interconnection boards, four substrate modules, and a connector for interface with the next level.

COMPUTER ASSEMBLY

The computer assembly is shown in Figure 6. It contains the central processor, memory, and power supplies. The configuration shown is for a 32-bit floating point machine with a 4K film memory.

It should be apparent by now that the SUMC is a significant step forward in aerospace computer packaging technology. It is estimated that the total active devices in the SUMC, exclusive of main memory and power supplies, is approximately 80 000 of which some 35 000 are associated with the ROM and approximately 16 000 are associated with the SPM. There are approximately 5700 logical gates (exclusive of the ROM and SPM) in a 32-bit floating point machine. The physical characteristics of the SUMC 32-bit machine are shown in Table 3.

TABLE 3. SUMC PHYSICAL CHARACTERISTICS

Construction:
LSI Multilayer alumina substrates Multilayer interconnection boards 4K memory
Weight: 2.49 kg (5.5 lb)
Volume: 3278 cm^3 (200 $in.^3$)
Power: 8 watts

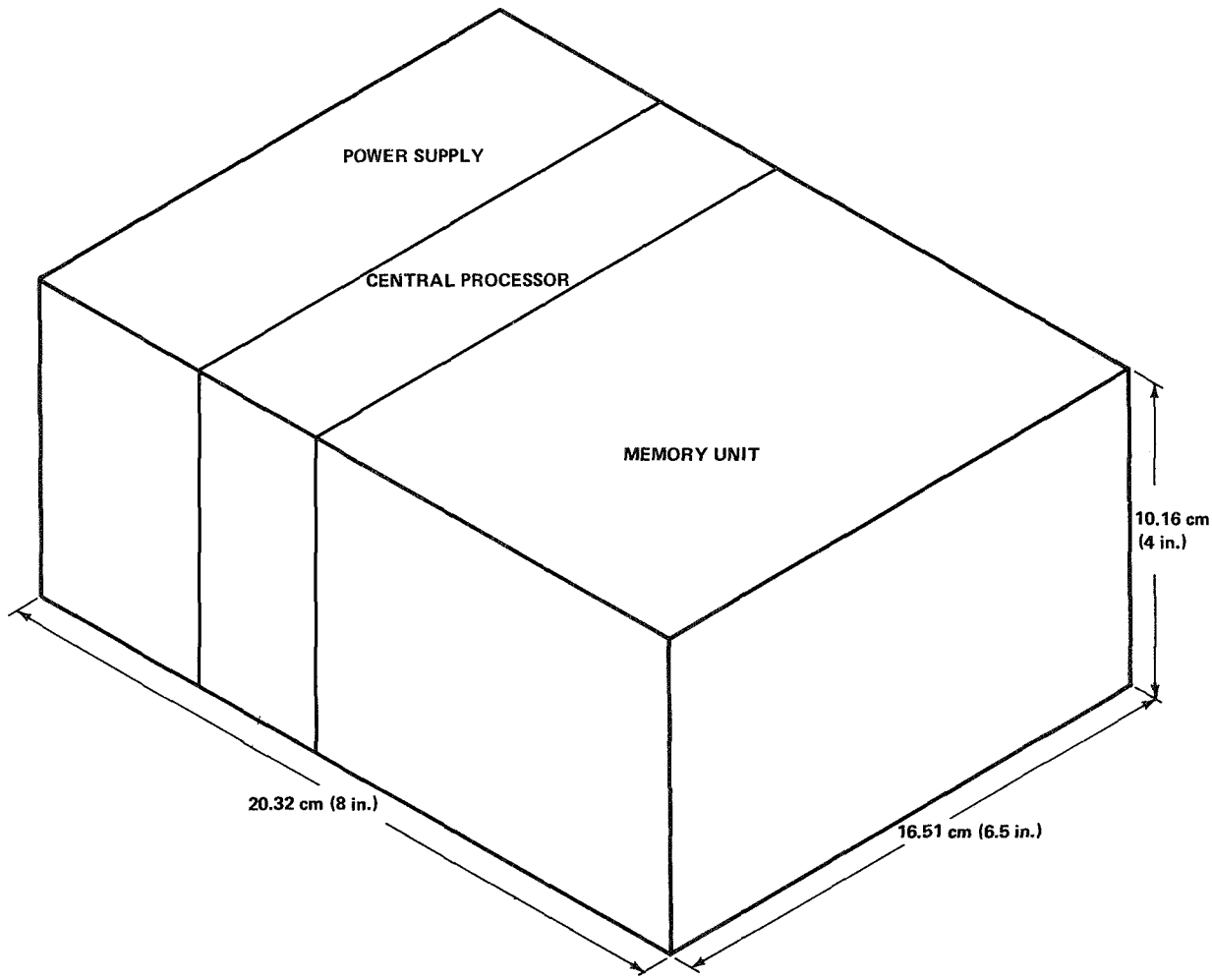

Figure 6. 32-bit SUMC with floating point.

Hardware/Software Trade Studies

In parallel with the SUMC hardware development, trade studies are being conducted, and the results are being fed into the SUMC design. These are as follows:

1. Hardware
    a. Instruction Set
    b. Word Length
    c. Word Format
    d. ROM Organization
    e. Number of Registers
    f. Interrupt Requirements
2. Software
    a. Compiler/Assembler Requirements
    b. Programming Safeguards
    c. Multiprocessing Techniques
    d. Fault Isolation
    e. Recovery Techniques
    f. Program Verification/Debug
3. Reliability
    a. Redundancy Techniques
    b. Multiprocessor
    c. Multicomputer
    d. Automatic Error Detection and Fault Isolation

SUMC Development Plan and Status

The development plan for the SUMC can be summarized briefly as follows:

1. The system and logic design will be completed by mid-1970.

2. A logic verification breadboard (using TTL) is being constructed and testing will be complete by mid-1971.

3. One set of LSI chips, in preliminary packages (i.e., without beam leads), is being procured and will have completed testing by late 1971.

4. Effort has been initiated to develop LSI C-MOS with beam leads. This effort should yield satisfactory results in time for prototype procurement.

5. Sufficient hardware will be procured/fabricated to construct an engineering prototype of a SUMC and to complete its testing by mid-1973.

The status of the SUMC effort at the present time is as follows:

1. A contract has been issued for two of the eight types of LSI chips; i.e., MRU and ACU. The design of the remaining types is 90 percent complete. Lack of funding has caused some delay in procuring the remaining LSI chip types.

2. The design of the logic verification breadboard is approximately 40 percent complete and it is being fabricated.

3. Packaging studies are being conducted.

It should be noted that the above development plan is based on acquiring adequate funding. If this does not occur, the schedules will be adversely affected.

CONCLUSION

The family of computers being developed by the Marshall Space Flight Center Computers Division represents a significant advance in the state-of-the-art of aerospace computers and thereby provides the capability to meet future mission requirements. The SUMC will provide a high degree of flexibility and reliability when applied in applications such as the Space Shuttle and Space Station.

MULTIPLEXED DATA BUS TECHNIQUES FOR ADVANCED AVIONICS SYSTEMS

By

W. O. Frost

INTRODUCTION

Astounding reductions in the size, weight, and volume of a complex avionics system such as that required for the Space Shuttle will result from medium scale integration/large scale integration (MSI/LSI) technology. However, experience indicates that a significant fraction of the weight of such a system is attributable to the wires, connectors, and associated mounting hardware required to interconnect the various physically separated elements of the system. To prevent such interconnections from becoming a disproportionately large fraction of the system size and weight, the merits of using multiplexing techniques for the transfer of data and command signals between the system elements are under consideration.

The use of multiplexing techniques for acquiring signals necessary to monitor system operation has been used by telemetry engineers for many years. However, point-to-point wiring has generally been used for the critical commands and operational signals flowing within an avionics system. The extension of multiplexing techniques to form an internal communication system for transfer of commands and operational signals, as well as monitoring signals, has by popular usage gained the designation "data bus techniques."

The following definition describes a data bus subsystem: a multiplexed signal collection and distribution arrangement with multiple input and/or output terminals interconnected by a shared transmission medium. The key words associated with such a subsystem are multiplexed data flow, multiple inputs and outputs, and shared transmission medium. A data bus subsystem has three essential elements. The bus controller supervises the flow of signals so that the multiple users do not interfere with one another. The transmission medium provides a shared path (or paths) for multiplexed supervisory and data signals, and data terminals process and route the signals to and from user subsystems and produce signals appropriate for the transmission medium.

In addition to possible savings in size and weight resulting from the elimination of wires, connectors, and associated hardware, two other potential advantages accrue from the use of multiplexed data bus techniques. First, it will simplify the initial installation of equipment because of a reduction in cabling requirements and will reduce the cost of later modifications because system changes can be made entirely within line replaceable units without impacting vehicle cabling. Secondly, gains in reliability may become possible, because with a marked decrease in interconnections, it becomes practical to use redundancy in the data bus subsystem. Thus, the single point failures inherent in conventional point-to-point wiring are eliminated.

GENERAL REQUIREMENTS

To properly consider a data bus subsystem design for a specific application, the design engineer needs a definition of data flow requirements. It is convenient to express this information in terms of a data flow model. This model provides a detailed description of each message path between physically separated elements of the avionics system. It includes information such as point of origin, destination(s), signal function, type of signal (analog, discrete, digital word, etc.) resolution, accuracy, occurrence statistics, and any special characteristics or requirements pertinent to data bus design and operation.

The design engineer also needs a description of those physical and environmental characteristics of the application that are pertinent to design of the data bus subsystem. These include location of user subsystems, cable lengths between locations, expected temperature variations and vibration levels at specific locations, and electromagnetic interference (EMI) characteristics. In addition, the design engineer needs descriptions of input/output characteristics of the various user subsystems pertinent to signal transfer operations to and from the data terminals.

Figure 1 shows a generalized representation of an advanced avionics system with signal flow serviced by a multiplexed data bus subsystem. One or more computers perform computational functions associated with guidance, navigation, control, display, checkout, etc. Various sensors and other subsystems such as the inertial measuring unit, propulsion systems, and control actuators perform their respective functions. The data and command signals handled by the data bus include discrete or proportional commands from the computers to various subsystems and sensor or subsystem inputs to the computer. However, it is important to notice that many signal paths do not involve the computers. Monitoring signals from various sensors and subsystems for telemetering and for onboard recording, signals for updating of status indications, and signal flow between elements of distributed subsystems are examples of message paths that may be independent of the computers.

DESIGN TECHNOLOGY

Given the general requirements described above plus specific system requirements such as weight limitation, power constraints, and reliability or failure criteria, the design engineer is prepared to consider the merits of numerous design alternatives for a multiplexed data bus subsystem. It is convenient to discuss the technology for such a design under the following categories: (1) transmission media; (2) signal design and detection; (3) synchronization, timing, and control; (4) user-subsystem interfaces; and (5) operational reliability.

Transmission Media

Numerous forms of transmission media have been suggested for use in data bus subsystems.

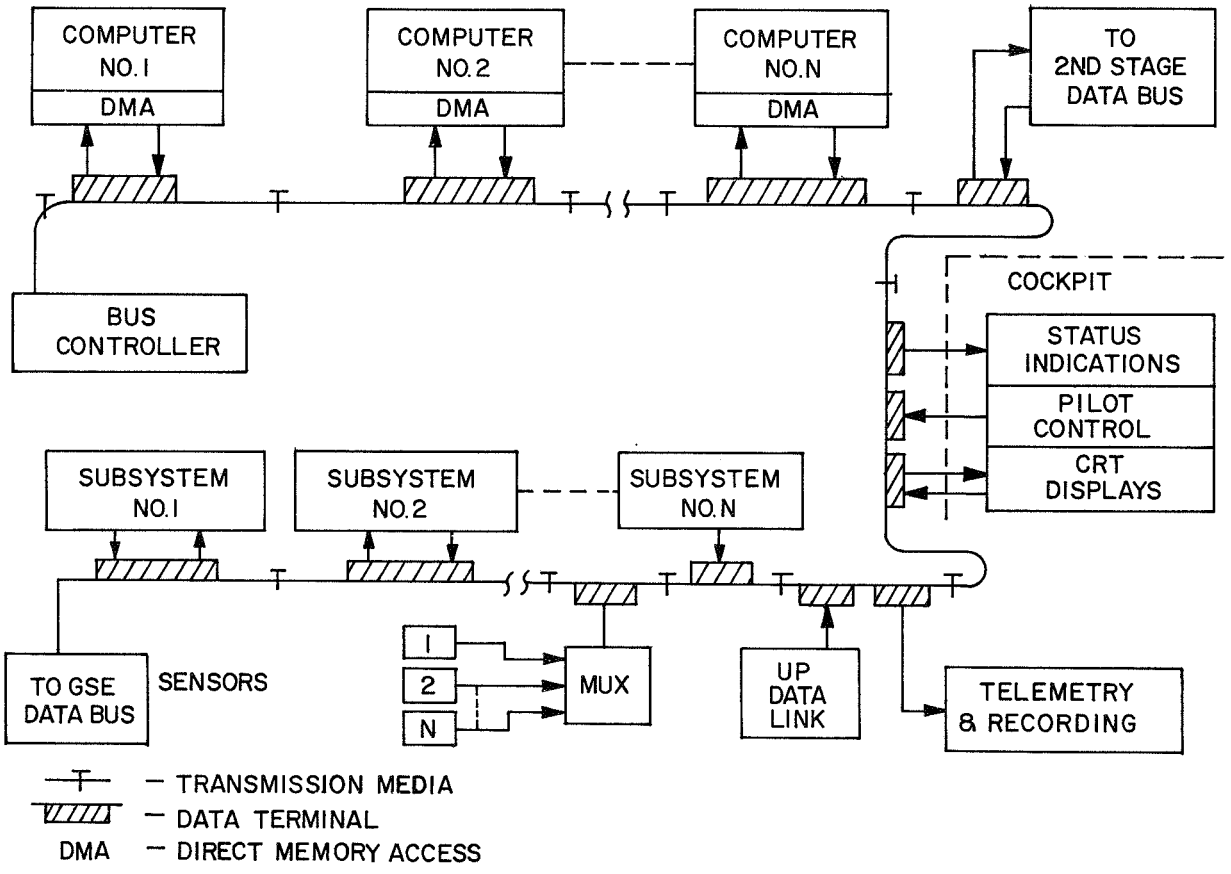

Figure 1. Integrated avionics system.

Among these are twisted-shielded pairs, coaxial cable, twin-axial cable, and triaxial cable. For transfer of digital signals at rates less than approximately 2 megabits, twisted-shielded pairs and twin-axial cable have received most prominent mention. These two are balanced arrangements that potentially can provide greater resistance to sources of low frequency interference.

The properties and parameters of a medium significant to a data bus design, in addition to interference susceptibility, include propagation delay and signal transfer characteristics such as amplitude, time, frequency, and phase characteristics. These properties typically vary as a function of loading, line terminations, signal form, and length of path, as well as medium form. Hence it is necessary to acquire test results under a variety of conditions to properly assess the potential of specific forms of media.

Signal Design and Detection

A second important technology category that requires careful consideration in the data bus design is the selection, generation, and detection of transmission signals. Three types of information must be transmitted; data/command information between various user subsystems, bus supervisory information, and the timing and synchronization information required for proper bus operation. Some of the considerations covered by this category are:

1. Type of multiplexing

2. Form of modulation

3. Spectral characteristics and bandwidth requirements of candidate signals

4. Signal generation, demodulation, and detection methods

5. Coding techniques

6. Message format arrangements

Both time division and frequency division multiplexing have merits for specific data bus applications. However, in applications such as the Space Shuttle, a digital time division arrangement is mentioned most often. The modulation techniques that have been proposed for bus applications include phase shift keying (PSK), amplitude shift keying (ASK), and frequency shift keying (FSK).

Synchronization, Timing, and Control

A third technology category critical to the multiplexed data bus design is the synchronization and control of bus operation. Considerations that fall into this category include:

1. Bus access control — Methods for supervision of multiplex operation so that the transmission medium can be shared without interference between user subsystems.

2. Message routing control — Methods for directing the routing of messages from the point of origin to their proper destinations.

3. Timing and synchronization — Methods for the timing and synchronization of transmission and message transfer operations such as modulation/demodulation, bit identification/detection, word or group identification, and bus/user subsystem transfers.

4. Programing — Methods and problems relating to the programing of data acquisition and distribution operations including both software and hardware techniques.

Studies of synchronization, timing, and control methods and problems should emphasize the capability of the data bus subsystem to flexibly adapt to changing requirements of the user subsystems. Careful consideration also should be given to the interaction with, and impact on, design and programing of user subsystems.

User-Subsystem Interfaces

Because of the variety of subsystems that must interface with the data bus subsystem, extensive study of bus/user subsystem interface and integration problems is appropriate. A myriad of electronic operations is required at each interface location. These may include modulation, demodulation, bit and word synchronization, detection, error checking, multiplexing, demultiplexing, data sampling and conversion, and buffering. Various subsystems may require different methods for information transfer such as synchronous or

non-synchronous and parallel or serial. Together with these diverse requirements, one must consider the merits of standardization of interface terminals or elements thereof. Standardization may reduce design costs and logistic requirements, but introduce limitations and constraints into the design. Physical considerations such as the packaging of interface elements and the electrical interconnections with user subsystems must also be considered at this point.

Operational Reliability

A final technology category of critical importance to the multiplexed data bus design is operational reliability. Typically the designer is given specific failure and reliability criteria along with test and maintenance requirements. A variety of alternatives are available to enhance these aspects of the design. These include parallel redundant arrangements such as circuit redundancy, triple modular redundancy with voting, and switchable redundant blocks. The design also may include self-checking features such as error-detection (or correction) coding, return verification of messages, periodic test message transfers, and time-dependent coding checks. He must give appropriate consideration to potential sources of interference such as EMI, common-mode signals, and power supply perturbations.

Test and checkout is an operational problem inherent in avionics systems. Hence, suitable methods and techniques must be derived for monitoring the operational readiness of the data bus subsystem including the status of redundant subsystem elements. A closely related consideration is problems and alternatives relating to the maintainability of the data bus subsystem.

CONCLUSIONS

Although multiplexed data bus techniques have been used for several years in the instrumentation and telemetry area, these applications have not approached the degree of complexity involved in proposed programs such as the Space Shuttle. In these applications, the data bus subsystem must interface with and function intimately with all elements of the avionics system. A commitment to a preferred design configuration must be made only after intensive study and analysis.

RELIABILITY EVALUATION OF BIPOLAR LSI MICROCIRCUITS

By

Leon Hamiter and Federico Laracuente

SUMMARY

Bipolar large scale integrated (LSI) circuits constructed with multilevel molybdenum-gold metallization were evaluated to identify and understand design and manufacturing weaknesses typical of these circuits, to determine their actual or most probable failure mechanisms, and to develop quality standards and screening criteria for the circuits.

The circuits tested were transistor-transistor logic built on a 3.175 cm (1.25 in.) silicon wafer and packaged in a 156-lead ceramic, glass, and metal package. Their functional configuration included logic gates, flip-flops, and shift registers.

The test program consisted of the following tests: static bias and high temperature, high temperature storage, temperature cycling, and operating life at 343.15°K (70°C) and 398.15°K (125°C). Several tests were also conducted to evaluate multilevel metallization and package reliability. The LSI circuits withstood the static bias with high temperature test and passed 6094 hours of storage at 398.15°K (125°C) without failure. In operating life tests, a total of 12 188 circuit-hours were accumulated with zero failures. The molybdenum-gold metallization system proved reliable in a temperature-humidity evaluation; however, complete failure was experienced with the epoxy-sealed 156-lead ceramic flat packs. Hermetically sealed packages with 28, 36, and 64 leads passed the tests. A redesigned 156-lead package successfully passed a later sequence of tests.

It can be concluded that bipolar LSI circuits using molybdenum-gold multilevel metallization can be designed, manufactured, and used reliably with improved performance in space systems. It is mandatory that manufacturers maintain stringent process controls, and effective quality assurance programs.

INTRODUCTION

With large scale integration came new problems and a new challenge for the reliability engineer, who has not yet solved all the problems associated with the older microcircuit technology. Added to his worries are multilevel metallization, interlayer insulation, metallization crossovers, functional testing, and environmental screening of extremely complicated LSI circuits.

In 1968, the Marshall Space Flight Center Quality and Reliability Assurance Laboratory initiated a program to evaluate the reliability of bipolar LSI circuits, and a contract was awarded to Texas Instruments with the following objectives:

1. Identify the failure mechanisms applicable to bipolar LSI technology.

2. Develop effective quality standards and controls and screening techniques to yield reliable LSI circuits.

3. Develop guidelines and format for preparing meaningful quality assurance specifications for LSI circuits.

This paper reports the significant results obtained from this program.

DESCRIPTION OF LSI CIRCUITS

It is difficult to quantitatively define large scale integration; however, it is generally accepted that an LSI circuit or array contains the equivalent of 100 gates or more. A more general definition states that large scale integration is the incorporation and interconnection of a large number of active and

passive elements (transistors, diodes, resistors, and others) built on a single silicon chip or wafer to function as an electronic system or subsystem.

The circuits used in the investigations and evaluations of this program are considered as large scale integrated circuits. The first level of fabrication is transistor-transistor logic, essentially the same as Texas Instruments Series 54 integrated circuit gates and flip-flops. The first level is fabricated in the same manner as conventional integrated circuits as shown in Figure 1.

The integrated circuit (IC) cells are insulated with layers of sputtered SiO_2 and "Silane" as shown in Figure 2. Silane is SiO_2 produced by a reaction between Silane gas and oxygen. The second level metallization consisting of layers of aluminum, molybdenum, and gold is applied for second level interconnection, and the process is repeated for the third level interconnection pattern. Interlevel connections or feedthroughs are made through windows cut in the insulation as shown in Figure 3.

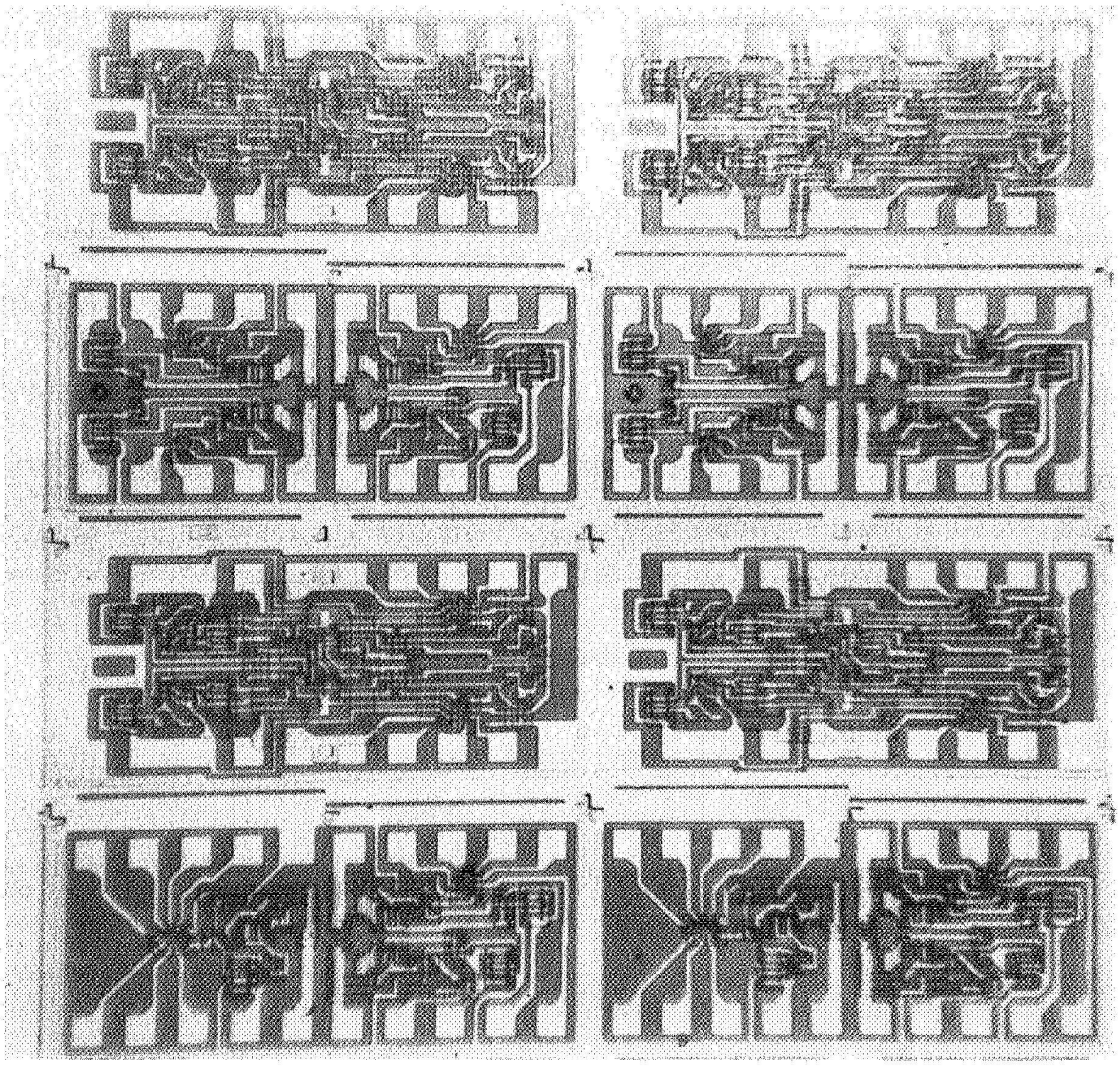

Figure 1. Lowest level of cells in LSI.

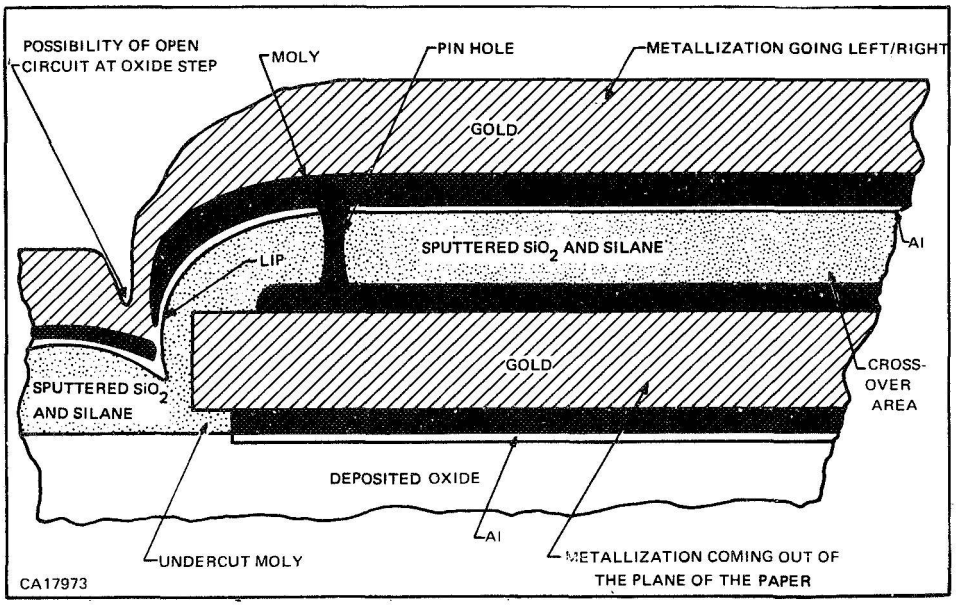

Figure 2. Cross section of LSI metallization and insulation.

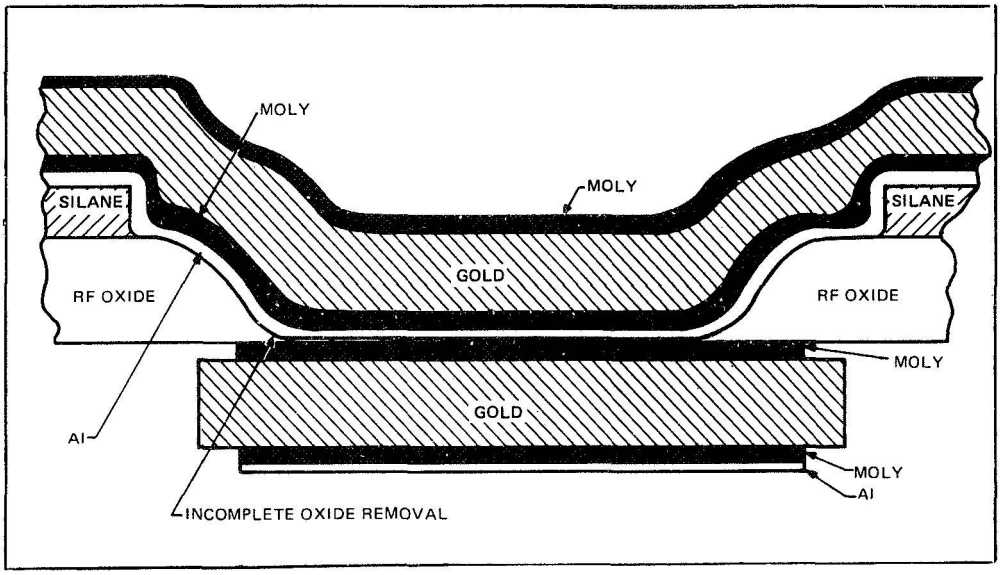

Figure 3. Cross section of interconnection feedthroughs.

The tested circuits were built on a 3.175-cm (1.25-in.) silicon wafer, as shown in Figure 4, and contained up to 200 gates (1800 transistors and resistors).

The test circuits were designated E30, E17, and TA00050, all packaged in a 156-lead flat package similar to that shown in Figure 5, except that it had a ceramic lid that was sealed on with epoxy.

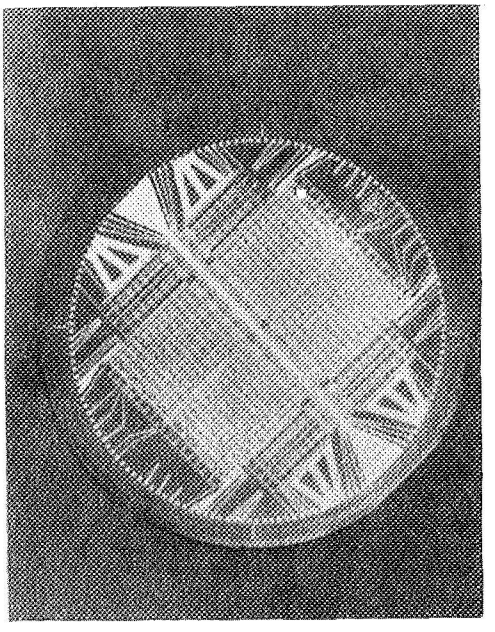

Figure 4. Complete LSI circuit.

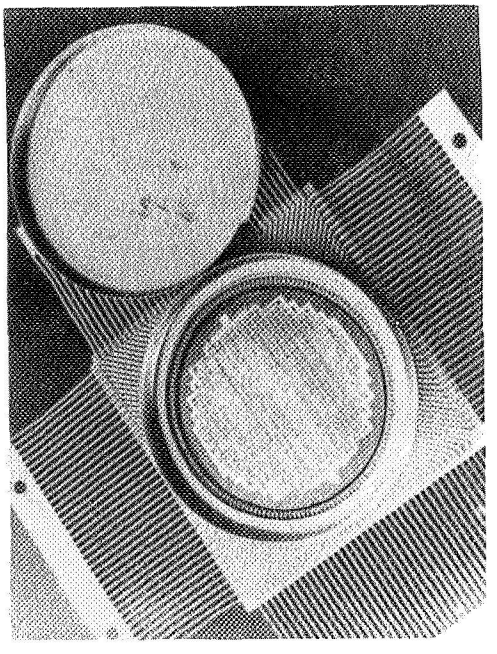

Figure 5. LSI circuit in 156-lead package.

TEST PROGRAM AND RESULTS

For this reliability evaluation, tests were selected that would detect design, manufacturing, quality, and functional defects. The prime purpose of the tests was to stimulate latent deficiencies to bring them to the point of failure or to enable detection through degradation. The tests in this program consisted of the following:

1. High temperature and static bias [500 hours at 358.15°K (85°C) and 500 hours at 398.15°K (125°C)].

2. High temperature storage at 398.15°K (125°C) for 6094 hours.

3. Shock-temperature cycling on five each of four types of packages (28, 36, 64, and 156 pins).

4. Temperature-humidity on multilevel metallization.

5. Intralevel leakage at 298.15°K (25°C), 323.15°K (50°C), 348.15°K (75°C), and 373.15°K (100°C).

6. Operating life tests for a total of 12 188 circuit-hours.

High Temperature and Static Bias

The objective of this test was to determine the effects of high temperature and static bias on multilevel metallization, ball bonds, repair wiring, and electrical performance. Two E17 test devices (a high speed, two-bit binary counter with 12 gates and 2 flip-flops) passed functional tests before and after exposure to 358.15°K (85°C) for 500 hours and 398.15°K (125°C) for 500 hours, both with a 2.4 volt bias and a Vcc of 5 volts.

High Temperature Storage

The purpose of this test was to evaluate the effects of high temperature on the performance of the LSI circuits. Two E17 devices were subjected to 398.15°K (125°C) storage for 6094 hours without failure.

Shock-Temperature Cycling

This test was performed to evaluate the ability of the LSI packages to withstand thermal shock and high temperature. The test sequence is shown in Figure 6. This proved to be a valuable test, since all the epoxy-sealed 156-lead packages failed. Thirteen redesigned packages have been subjected to a modified test sequence (Fig. 7), and the results are very encouraging.

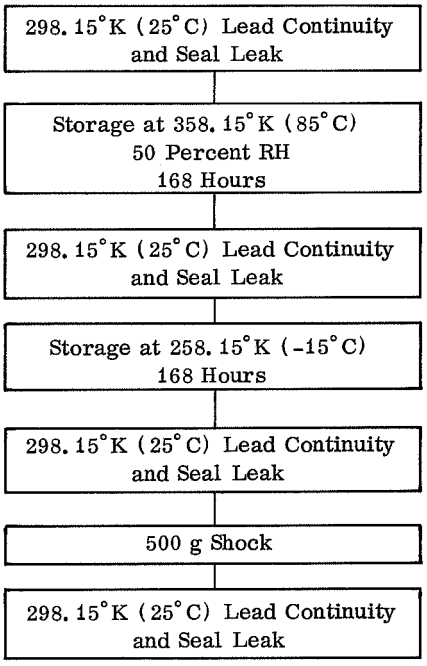

Figure 6. Test sequence for shock temperature cycling.

Temperature-Humidity on Multilevel Metallization

This test was performed to determine the effects of high temperature and humidity on multilevel metallization. Two samples each of two different metallization systems were evaluated: tungsten gold and molybdenum gold. After initial resistance measurements, the test devices were subjected to 343.15°K (70°C) and increasing relative humidity (RH) in the following steps: 168 hours 50 percent RH, 168 hours 75 percent RH, 168 hours 85 percent RH, and up to 1680 hours at 95 percent RH. After each step, the devices were checked electrically for opens or shorts and were visually inspected for deterioration. The tungsten-gold metallization showed slight corrosion after 672 hours of test, and severe corrosion was observed after 840 hours. The molybdenum-gold

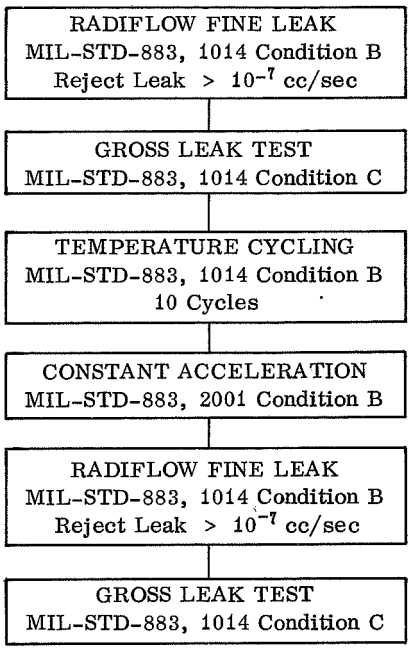

Figure 7. Test sequence for package evaluation.

metallization devices were not affected until after 2184 hours of test, demonstrating superiority over tungsten gold. These tests also emphasize the need to protect LSI circuits in a hermetically sealed package with a dry interior.

Intralevel Leakage

To obtain a detailed picture of intralevel leakage current as a function of temperature and voltage, six test vehicles were tested at 298.15, 323.15, 348.15, and 373.15°K (25, 50, 75, and 100°C). A plot was made of intralevel current as a function of temperature and voltage between sections of metallization. The results indicate that intralevel leakage current is not a significant reliability problem.

Operating Life Tests

The operating life test had three objectives:

1. Isolate failure mechanisms that depend on time.

2. Obtain data on performance degradation as a function of time.

3. Predict failure rate (or MTBF) of the device.

The five TA00050 test devices were subjected to 336 hours of life test at 398.15°K (125°C). There were no failures; however, the devices were damaged, and the test was discontinued after 336 hours. One E30 device was tested for 6855 hours at 343.15°K (70°C) and five other E30's were tested for 4984 hours at 343.15°K (70°C). All E30 flip-flop inputs and gate inputs were set at 2.4 volts dc and were driven by a 2.0-volt, 5-MHz clock pulse.

The results of these tests are summarized and tabulated in Table 1, which also includes the results of Static Bias and Storage Life Tests. There were no failures during these tests. On the basis of 35 455 circuit-hours with zero failures, one may calculate a circuit failure rate of less than 2.6 percent/1000 hours at a 60 percent confidence level. Since no operating failures were observed, we did not increase our knowledge of failure mechanisms; however, based on our experience with integrated circuits, we can infer what the failure mechanisms would be for LSI.

FAILURE MECHANISMS

The failure mechanisms for bipolar LSI technology can be logically arranged into three classes: (1) those associated with silicon wafer fabrication by normal IC technology; (2) those associated with the multilevel interconnection process; and (3) those associated with the package and interconnection from wafer to package terminals.

Wafer Failure Mechanisms

Failure mechanisms associated with the LSI wafer process are for the most part the same as those for a standard IC chip and are summarized below.

1. Failures Related to Bulk Material
   a. Dislocations
   b. Stacking faults
   c. Twins
   d. Growth strains
   e. Interstitial precipitation centers
2. Surface Related Failures
   a. Inversion
   b. Pinholes in oxide
   c. Oxide undercutting
   d. Oxide scratches

TABLE 1. SUMMARY OF LIFE AND STORAGE TESTS ON BIPOLAR LSI

Test Conditions	Device Type	Number Devices	Test Hours	Failures	LSIC, Hours
Operating Life Test @ 398.15°K (125°C)	TA00050 (Shift Register)	5	336	0	1 680
Operating Life Test @ 343.15°K (70°C)	E-30 (Logic)	1	6855	0	6 855
Operating Life Test @ 343.15°K (70°C)	E-30 (Logic)	5	4984	0	24 920
Static Bias 500 Hours @ 358.15°K (85°C) 500 Hours @ 398.15°K (125°C)	E-17 (Logic)	2	1000	0	2 000
Storage Life @ 398.15°K (125°C)	E-17 (Logic)	2	6094	0	12 188
			TOTALS	0	47 643

3. Metallization

   a. Undercutting

   b. Peeling-delamination

   c. Scratches

   d. Improper thickness

Multilevel Interconnection Failure Mechanisms

There are four basic ways that the multilevel interconnections can fail: (1) by shorting either interlevel or intralevel; (2) by openings in metallization at crossover steps or at interlevel feedthrough connections; (3) by high sheet resistance of metallization; and (4) by excessive interlevel or intralevel leakage currents. These failure mechanisms are summarized below.

1. Interlevel Shorts

   a. Oxide pinholes resulting from particulate contamination.

   b. Mask defect causing an undesired removal.

2. Intralevel (Interfacial) Shorts

   a. Mask defect causing incomplete metallization removal.

3. Open at Crossover and Feedthrough

   a. Nonuniform metallization at crossover.

   b. Incomplete oxide removal at feedthrough or contamination.

4. High Leakage Current

   a. Small pinhole or pores in the oxide.

   b. Contamination at oxide interface.

INTERLEVEL OR INTRALEVEL SHORTS

The mechanism that leads to interlevel shorts is oxide pinholes at metallization crossovers. The usual cause of oxide pinholes is particulate contamination introduced during the oxide deposition process. A typical insulation deposition process requires the formation of two separate layers of insulating material. The first layer consists of about 1×10^{-6} m (10 000 Å) of radio frequency (RF) sputtered SiO_2 and the second layer consists of about 5×10^{-7} m (5000 Å) of silane (SiO_2 produced by a reaction between silane gas and oxygen). This two-layer process tends to minimize the occurrence of short-producing pinholes by reducing the probability that pinholes in the two independently deposited oxide layers will be coincident.

The principal causes of intralevel shorts are incomplete metal removal and mask defects. Of the two types of shorts (intralevel and interlevel), interlevel shorts are the most common.

OPENS AT CROSSOVERS AND FEEDTHROUGHS

When oxide is placed over Mo-Au-Mo metallization, there is a tendency for a lip of oxide to build up at the edge of the metallization. This lip can cause the metallization that is deposited on top of the oxide to build up nonuniformly at the lip and, in some cases, leads to an open circuit or thin metallization (a condition conducive to electromigration) at the oxide step.

Open circuits, or high contact resistance at feedthrough holes (i.e., holes to permit interconnection between metallization located on different levels) can be caused by incomplete oxide removal. The feedthrough hole shown in Figure 2 is wider at the top than it is at the bottom. This is because silane etches faster than RF-sputtered oxide. High contact resistance could also be caused by contamination at the interface, but this problem has not been observed to date.

HIGH SHEET RESISTANCE OF METALLIZATION

The nominal sheet resistance of the Mo-Au-Mo metallization is 0.05 ohms per square. However, to achieve this value of sheet resistance, it is necessary to bake or "anneal" the metallization at 773.15°K (500°C) briefly to drive out the inert gases that are trapped within the metal during the deposition process. If this "annealing" is unsuccessful, the sheet resistance can become excessively high causing abnormally large voltage drops in the metal leads. Incorrect sheet resistance of the metallization can also create conditions that are conducive to current-induced mass transport.

LEAKAGE CURRENT

Failure mechanisms that cause excessive leakage current, either intralevel or interlevel, have not proven to be very significant up to this point in the development of LSI technology. This is particularly true of interfacial leakage current. Interlevel leakage current, when caused by small pores or pinholes, can usually be "cured" by burning them open. After this curing treatment, the interlevel leakage is either acceptably small or unacceptable. The long-term effect of burning-out minor leakage defects is presently under evaluation.

Package Failure Mechanisms

The packaging system to be used with LSI technology is not yet fully developed, but it appears very likely that a design using a 156-pin ceramic package will be employed. Test results for an 80-pin ceramic package (MSI) suggest that a rugged and hermetic package for LSI should be possible using a ceramic design. Basically, the package will be composed of two parts, which are a flat ceramic base with gold plated lands and a ceramic lid. The slice is mounted on the ceramic base with epoxy and connections are made between the slice bonding pads and the metal lands. The lid is attached to a metallized ring on the ceramic base with solder and the metal lead frame is brazed to the metallized lead portion of the base that is not covered by the lid.

Although there is not a great deal of failure data for a large ceramic package, the following failure modes should be applicable:

1. Failure to seal lid to the metallized ceramic (hermeticity failure).

2. Failure of ball or stitch bonds to make proper contact (open circuit or high resistance).

3. Rupture of the ceramic base or lid (hermeticity failure).

The mechanisms that lead to these failure modes are related to processing errors, but at this time, there is insufficient data to clearly define what these failure mechanisms might be. However, based on experience to date, the following failure mechanisms are possible.

1. Hermeticity Failures

a. Pinhole in seal because of improper handling or epoxy contamination.

b. Crack in ceramic base or lid caused by stresses induced during application of epoxy seal.

2. Continuity Failures

a. Loose connection between lead frame and metal land because of improper brazing operations.

b. Thermocompression ball bond faulty because of contaminant on metal land or incorrect bonding procedure (i.e., wrong temperature or pressure).

c. Stitch bond faulty because of incorrect bonding procedure.

Relative Contribution to Failures

Listed below is a comparison of the relative contribution of each class of failure mechanisms to the total number of failures. The rationale for this particular breakdown is based on the maturity and complexity of the technology required to produce a completed slice, a multilevel metallization interconnection system, or a multipin ceramic package.

Class of Failure Mechanism	Percent Total Failure	Remarks
Slice	30	
Multilevel	50	Including repair wiring
Package	20	

The technology required to produce a multilevel interconnection system is very complex and is in the process of being developed. Consequently, it is expected that multilevel failures will predominate at least during the pilot production. Slice

processing technology is well developed but is quite complex. In contrast, the ceramic package technology is relatively new but is not very complex when compared to slice technology. The net effect is that the relative contribution of slice and package failures is not expected to be significantly different. The small difference in percent of contribution indicates that the slice, because of its complexity, will probably cause a few more failures than the package.

It is expected that this failure contribution breakdown will change as the LSI technology develops.

CONCLUSIONS

System reliability increases with a decrease in the number of parts used in the system, provided individual part reliability remains unchanged. Present LSI technology provides the means to produce complex LSI circuits that have a reliability comparable to the reliability of conventional microcircuits. Thus, LSI circuits promise a significant improvement in reliability by reducing the number of total parts.

The negative side of the above-mentioned concept is that with increased complexity, the number of pins and internal interconnections increases, thus degrading the reliability of the LSI package. This tendency towards degradation admittedly exists; however, any degradation that might otherwise occur is offset by the fact that the interconnections made inside an LSI package are more uniform, are of higher quality, and are produced under much tighter controls than those made by other means when discrete parts are employed.

Our evaluations indicate that the failure rate of today's LSI packages is equivalent to or lower than the failure rate of conventional integrated circuits. This is primarily attributed to the more stringent process controls that are a necessity for reasonable yield. Therefore, it is concluded that:

1. LSI can be successfully applied to the development of high performance, long life, electronic systems.

2. The impact of LSI on the electronics industry is limited only by human ingenuity; however, new packaging and testing techniques are required before full exploitation can be expected.

3. An LSI circuit offers a failure rate that is lower than the failure rate of an equivalent circuit built with discrete parts or integrated circuits.

4. High reliability LSI circuits for space systems require stringent design standards, strict process and quality control, good workmanship, and effective screening; but the potential benefits of improved performance and reliability are overwhelming.

MICROCIRCUITS, 10- TO 15-YEAR SPACE MISSIONS

By

M. F. Nowakowski and F. Villella

ABSTRACT

This paper discusses the technology necessary to determine whether microcircuits will satisfy performance requirements for 10- to 15-year space missions.

Large scale integration/medium scale integration (LSI/MSI) techniques are discussed, and the advantage of system reliability in keeping circuit complexity within a single silicon chip or wafer to function as an electronic system or subsystem is discussed. Redundancy, radiation tolerant devices, and rigorous in-process control and screening tests are also discussed with particular emphasis on how a microcircuit shall be controlled and how much testing must be done to assure the successful accomplishment of these missions.

INTRODUCTION

The realization of maximum useful payload along with optimum reliability in future space systems having long term operational requirements such as the Space Shuttle, Space Station, and Interplanetary Vehicles will depend largely upon the extent to which reliable high functional density microcircuits can be developed and used.

Today's technology has advanced to the point where it is feasible to manufacture complex microcircuits with the degree of reliability necessary to achieve 10- to 15-year space missions. However, new concepts for packaging, assembly, and system design must be developed in such a manner as to keep pace with the rapidly increasing complexity of the microcircuit.

As these microcircuits become more and more complex, minor variations in the processing that had previously been ignored in simple circuits must be controlled to a much greater degree since the significance of these variations increases with the complexity of the microcircuit. In addition to these tighter process controls, it is evident that new controls and analytical tools must be developed and employed.

Present screening concepts will also have to be reevaluated. Test methods and techniques must be devised in order to verify or extrapolate with a high degree of confidence the capability of these devices to operate in a space environment for these extended time periods.

LARGE SCALE INTEGRATION

Large scale integration (LSI) is the manufacture of a large number of active and passive electronic elements on a single semiconductor wafer. The elements and their interconnections comprise a completely functional system or subsystem.

Medium scale integration (MSI) utilizes the same technology employed in LSI but is less complex. The present trend is toward development of "standard" MSI devices for high volume production; whereas, the LSI devices will be manufactured primarily as low volume or "custom" units. Only LSI is discussed here since developments and improvements in this area may be easily applied to MSI types.

The highest functional density of LSI is obtained using the metal-oxide-semiconductor (MOS) technique. This is because the MOS transistor requires a considerably smaller area and fewer elements per function than is required using the bipolar technique. Also, MOS LSI requires only a single level of metallization interconnections as opposed to the two or three levels required for equivalent bipolar LSI.

As expected, MOS LSI provides a considerably greater reduction in power consumption than is possible for an equivalent bipolar LSI. However, the long term stability of MOS LSI is questionable, and its resistance to radiation encountered in a space environment must be improved. The controls imposed by Line Certification along with improved technology

should solve the stability question, and it is expected that suitable design and packaging techniques will minimize the radiation effects to a level acceptable for long term manned space flight applications.

One of the major problems encountered to date with both MOS and bipolar LSI has been the packaging. Some devices require up to 150 leads to connect the LSI wafer to the "outside world." This requirement for a large number of leads in a relatively small package has created significant hermeticity problems that have not yet been satisfactorily resolved. Entirely new techniques may have to be developed to overcome this situation. One approach that appears to have good potential is the application of a passivation layer over the entire wafer including the metallization; such a development may completely preclude the necessity for hermetic packages.

Present data indicate that another major problem with complex microcircuits is the internal interconnecting system. New developments such as spider, wire, ribbon, and especially beam leads offer a scheme by which many of the inherent interconnection problems may be solved. The beam lead system affords the advantage of mono-atomic (gold-gold) bonds that substantially reduce or eliminate problems resulting from electromigration.

LSI technology is relatively new, and its usage is somewhat limited to date; however, substantial effort is being put into its development, and there is little doubt that it will be available in appreciable quantities in many forms and functions in the very near future.

The advantages of LSI for use in space flight hardware are very impressive. Extensive use of LSI in the Space Shuttle and other new long term space programs will provide weight reductions of at least 10:1 with corresponding reductions in volume and power consumption. Maintenance will be greatly simplified, since each LSI component will exist as a complete system or subsystem in itself. Trouble-shooting below the subsystem level will be virtually eliminated. With the reliability of the LSI component firmly established, the level of confidence of the system will be much higher than presently exists because of the fewer components and the resulting decrease in the number of external connections.

REDUNDANCY

In the past, redundancy has been applied at the component, circuit, subsystem, or system level. With LSI, redundancy at the component and system or subsystem level will be synonymous, and extensive redundancy with little sacrifice in power and weight will be possible. In fact, the LSI device can conceivably include its own redundancy on the same wafer.

The degree of redundancy made available through extensive use of LSI and the degree of reliability expected from well designed, manufactured, and tested LSI components can be combined to provide assurance of electronic hardware easily capable of 10- to 15-year operation in a space environment.

LINE CERTIFICATION

Presently, it appears that reliability enhancement through adequate and consistent process controls can be achieved using the Line Certification approach. In addition to providing more reliable microcircuits, Line Certification should provide more consistent quality and reliability and higher yields.

Line certification consists of a detailed evaluation of key process steps used in the manufacture of microcircuits. Each step is certified only upon implementation of proper and adequate controls over the materials and techniques. These process steps include:

1. Substrate characterization — The preparation of substrates (i.e.; silicon, silicon epitaxy, etc.) in or on which active and passive elements are to be fabricated.

2. Surface passivation — This includes the growth and/or deposition of any layer on the surface of the substrate for the purpose of fabricating functions, passivating the surface, or making a dielectric such as for field effect devices.

3. Patterning — A process step that includes the techniques and materials involved in opening

windows in passivating layers (such as making junctions or contacts) and forming metal interconnect patterns.

4. Junction formation — This includes the materials used in forming p-n junctions, gas flow rates, furnace temperature, dopant concentration, and diffusion time. All these factors are necessary to control the electrical characteristics such as breakdown voltage, speed, and gain of the microcircuit.

5. Metallization — This includes operations and materials used in fabricating the conductive network on the surface of the passivating layer for the purposes of making active contact to elements and interconnecting them on a monolithic circuit.

6. Interconnecting bonding — This process step includes those materials, controls, and techniques involved in connecting metallized, mounted, monolithic circuits from their bonding pads to the output leads of the protective package.

7. Sealing — The step in the process that includes the sealing of the circuit package after pre-seal inspection.

The manufacturer must also demonstrate the capability to continuously maintain these controls at the level certified.

In the future, certification requirements of lines used to manufacture complex microcircuits may include sophisticated analytical tools such as a scanning electron microscope, a scanning infrared microscope, auger-spectroscopy, X-ray topography, and noise analysis.

AUTOMATIC VISUAL INSPECTION

In addition to the line certification techniques described above that presuppose near-absolute controls on the manufacturing processes of the microcircuits, steps such as automatic visual inspection, as well as the most vigorous manual visual inspection, will have to be performed. This can be considered one of the most important examinations of the microcircuit in achieving a high degree of reliability assurance.

As technology progresses and the complexity of LSI circuits increases, automatic visual inspection must become a reality. The complexity will be such that performance of this task manually, even with inspection personnel of the highest caliber, will be almost impossible. Automatic visual inspection will become especially important when a high degree of confidence is expected and when relatively high volumes of LSI microcircuits are involved.

Since most LSI microcircuits contain regular patterns and a more-or-less uniform layout, automatic visual inspection will lend itself to this task with significantly fewer defective devices proceeding to the next process step. Arthur D. Little, Inc. is currently conducting studies and developing equipment for an automatic visual inspection station under contract to NASA/Electronics Research Center. Three methods have been explored: the Scanning, Fourier Transform, and Space Filtering techniques. Presently, the Space Filtering technique seems the most suitable and accurate method for microcircuits. It is expected that manual visual inspection will also continue to have an important role, especially for low power gross visual internal inspections.

RELIABILITY TESTING

Unless innovations in accelerated reliability verification techniques can be developed, life testing will, at best, require approximately 7 years to verify a capability of 10- to 15-year reliable operation. It is obvious that life tests requiring such long periods would be incompatible with hardware development cost and schedule constraints. Since reliability verification cannot be accomplished in time to meet program schedules, design and process controls again are of prime importance. This does not imply that benefits and useful data cannot be obtained from life tests of several thousand hours. Such life testing would provide information on parameters and, consequently, processes that require more stringent controls to assure the circuit stability.

SCREENING

Since it may be impractical to demonstrate the reliability of LSI microcircuits through testing, rigorous screening techniques must be utilized to remove early failures and devices exhibiting instabilities that may limit their performance over 10- to 15-year operating times. However, the primary requirement is that they be designed and controlled by rigid standards.

One of the greatest factors limiting LSI performance and reliability is the protection of the circuit. Major innovations are necessary to develop suitable protection or a package capable of meeting the environmental requirements of space flight application. It is estimated that the package must withstand the following types of environments:

- Temperature shock and cycling
- High temperature storage
- Constant acceleration
- Mechanical shock and vibration
- Barometric pressure
- Moisture resistance
- Solderability (weldability)

After exposure to these environments, the package must remain hermetically sealed, with the integrity of the leads maintained and the LSI circuit completely operational.

Since it is not possible to build a perfect circuit or even an acceptable circuit on every try, it is necessary that each circuit pass rigid screening tests and inspections. An LSI circuit of good design and manufactured under rigid process controls should be capable of meeting these requirements and should then demonstrate the necessary reliability over the required operational lifetime of the system.

The following screening table will provide a foundation for screening LSI circuits to meet today's requirements. As the techniques are improved and new ones are developed, they can be incorporated, and the table can be suitably modified.

- Die or wafer inspection — 200 X minimum
- Precap inspection — 40 X minimum
- Temperature cycle — 20 cycles, 338.15 to 423.15°K (65 to 150° C)
- Temperature storage — maximum rating — 168 hours
- Constant acceleration — 20 000 g — Y1 axis
- Hermetic seal
- Electrical tests at 298.15°K (25° C) — read and record critical parameters
- High temperature and backbias at maximum temperature for 48 hours
- Electrical tests at 298.15°K (25° C) — read and record or go/no-go
- Burn in — 240 hours at rated temperature and power
- Electrical tests —
  1. Read and record critical parameters
  2. Reject devices that exhibit parameter drift greater than:
     a. Logic levels + 10 percent
     b. Leakage current
        (1) Low levels + 10 times initial
        (2) High levels + 20 percent
- Hermetic seal — fine and gross
- Radiographic inspection

New techniques must also be developed to determine and remove time-dependent failures. Techniques such as fast-scan infrared microscopes may be used to detect anomalies that exist but are not detectable through functional measurements. Possibly, test patterns should be developed to reveal subtle failure mechanisms such as those occurring in actual LSI circuits, making them questionable after having passed rigid screening tests.

All of these aspects of testing must be investigated in depth to achieve the required goals.

CONCLUSIONS

The future of LSI in extended space flight hardware appears very promising and will depend primarily on the degree of cooperation and commitment the semiconductor manufacturers and the

systems designers are willing to extend toward obtaining the goal. A large step in this direction is the favorable response and cooperation that has been received from a number of the leading semiconductor manufacturers in implementing the Line Certification Program.

Recent advances indicate that problems in areas such as packaging, interconnections, process controls, and design of LSI microcircuits are rapidly being solved; however, additional developments to adapt the system design to LSI microcircuit technology must be conducted.

The design engineer must accustom himself to designing systems at the system level rather than at the discrete part or component level, as is employed with today's technology. It is expected that this challenge will be met, as evidenced by the new system design concepts currently under development.

One of the major questions remaining is: How do we demonstrate reliability with a high degree of confidence? Confidence levels have not been established for long term operational life of the LSI microcircuits; however, with additional development in the above areas, it is believed that the necessary level for long term, 10- to 15-year, space missions can be achieved.

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APPROVAL

RESEARCH ACHIEVEMENTS REVIEW
VOLUME III REPORT NO. 11

The information in these reports has been reviewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. These reports, in their entirety, have been determined to be unclassified.

These reports have also been reviewed and approved for technical accuracy.

F. B. MOORE
Director, Astrionics Laboratory

D. GRAU
Director, Quality and Reliability Assurance Laboratory

UNITS OF MEASURE

In a prepared statement presented on August 5, 1965, to the U. S. House of Representatives Science and Astronautics Committee (chaired by George P. Miller of California), the position of the National Aeronautics and Space Administration on Units of Measure was stated by Dr. Alfred J. Eggers, Deputy Associate Administrator, Office of Advanced Research and Technology:

"In January of this year NASA directed that the international system of units should be considered the preferred system of units, and should be employed by the research centers as the primary system in all reports and publications of a technical nature, except where such use would reduce the usefulness of the report to the primary recipients. During the conversion period the use of customary units in parentheses following the SI units is permissible, but the parenthetical usage of conventional units will be discontinued as soon as it is judged that the normal users of the reports would not be particularly inconvenienced by the exclusive use of SI units."

The International System of Units (SI Units) has been adopted by the U. S. National Bureau of Standards (see NBS Technical News Bulletin, Vol. 48, No. 4, April 1964).

The International System of Units is defined in NASA SP-7012, "The International System of Units, Physical Constants, and Conversion Factors," which is available from the U. S. Government Printing Office, Washington, D. C. 20402.

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